



1/217

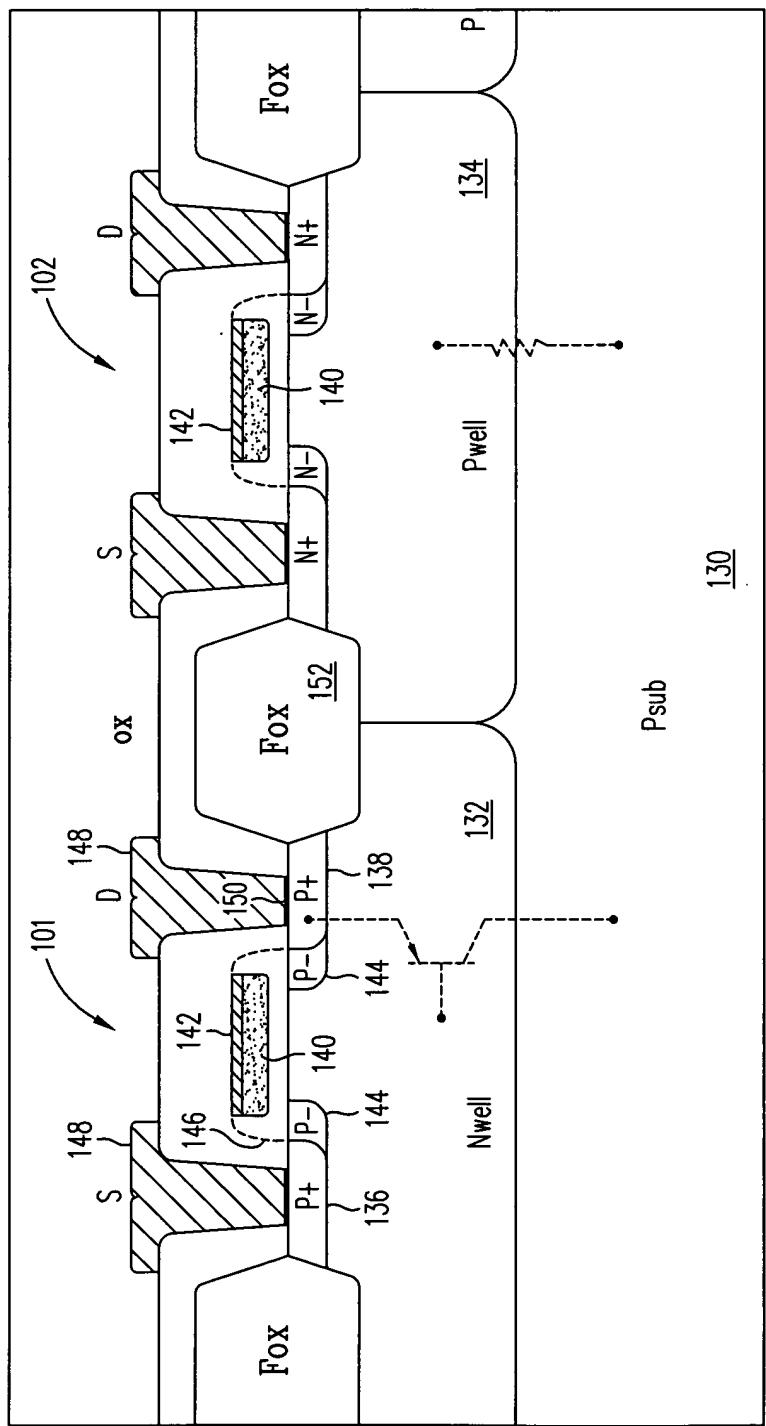


FIG. 1A
(Prior Art)

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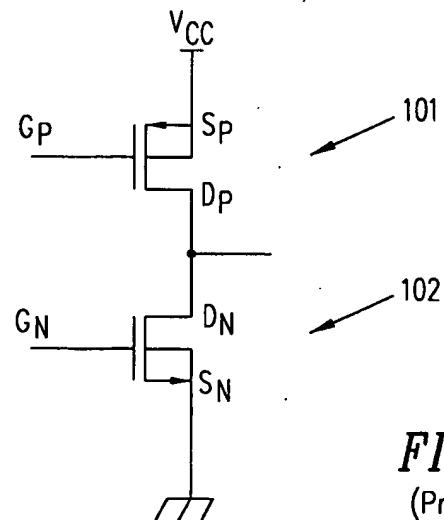


FIG. 1B
(Prior Art)

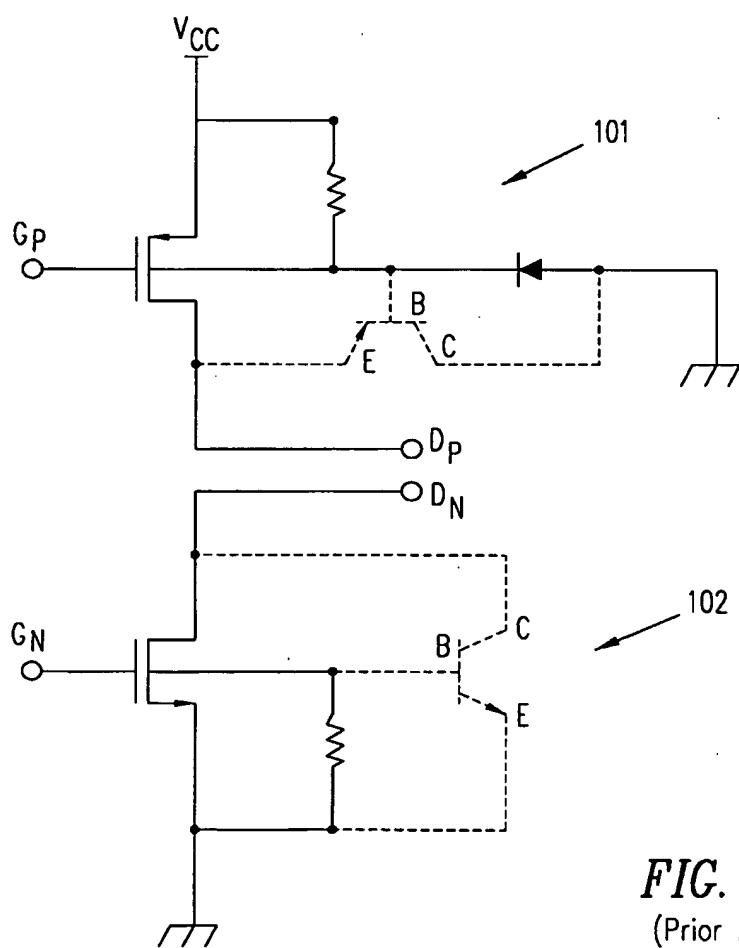


FIG. 1C
(Prior Art)

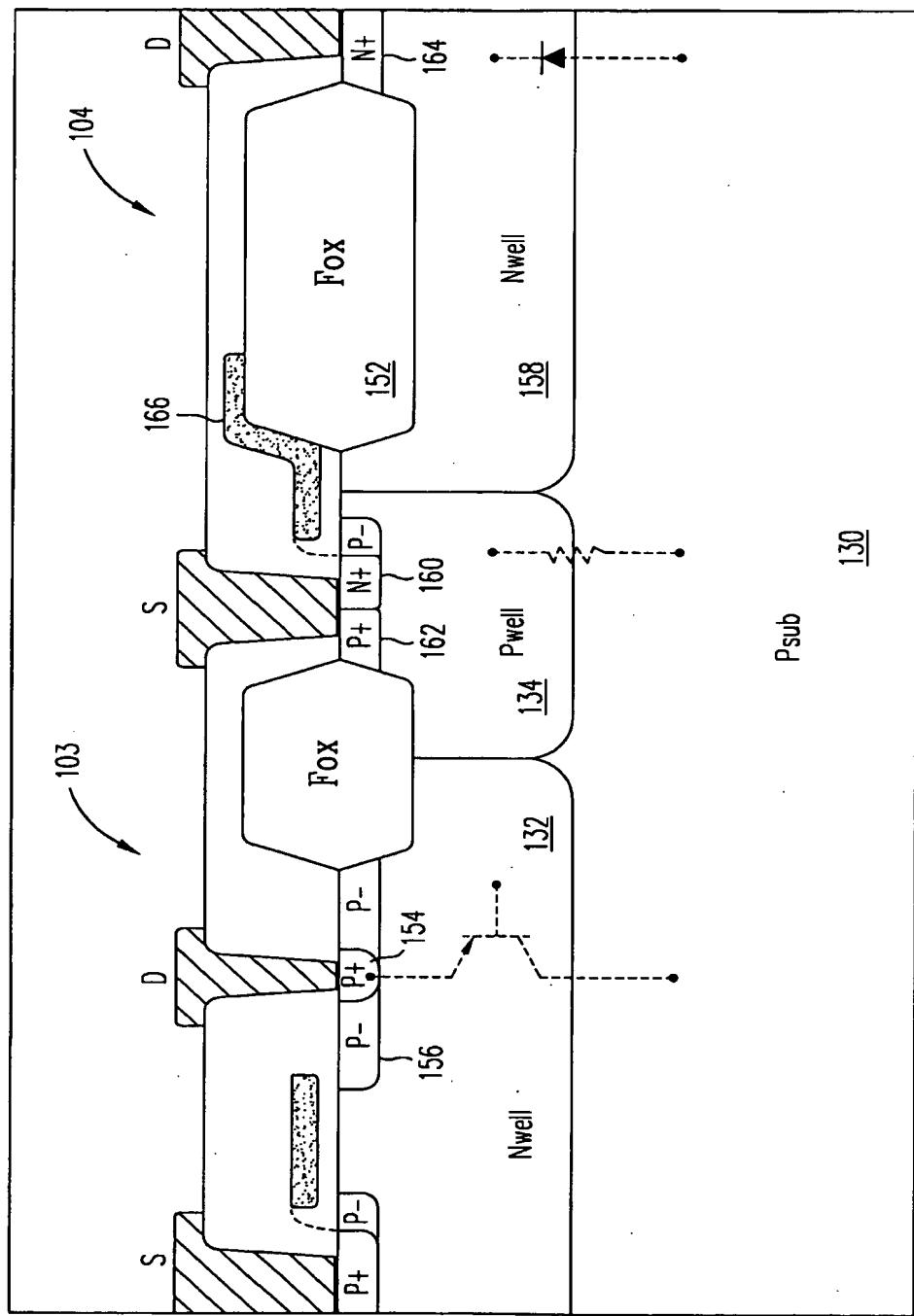
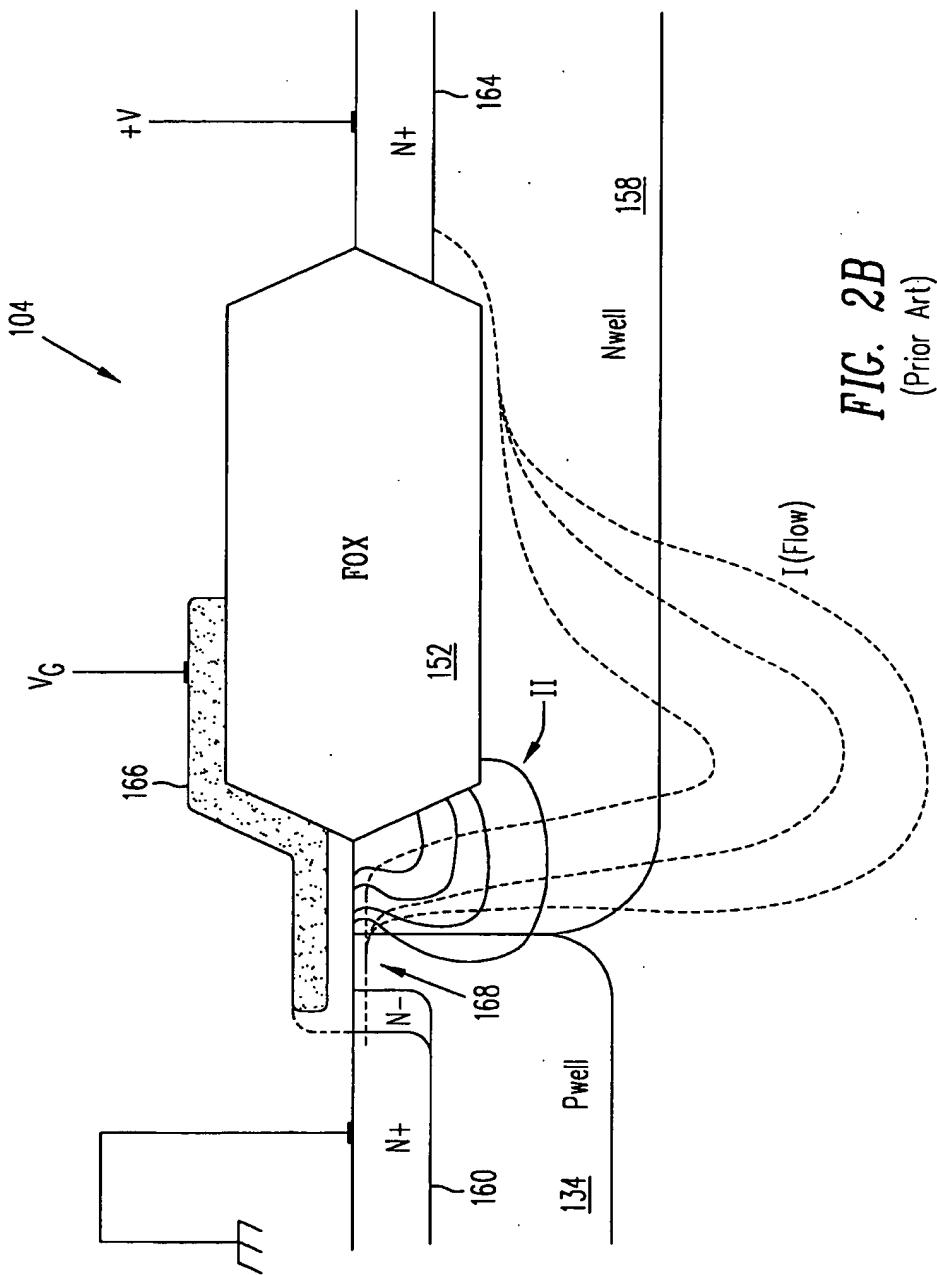


FIG. 2A
(Prior Art)



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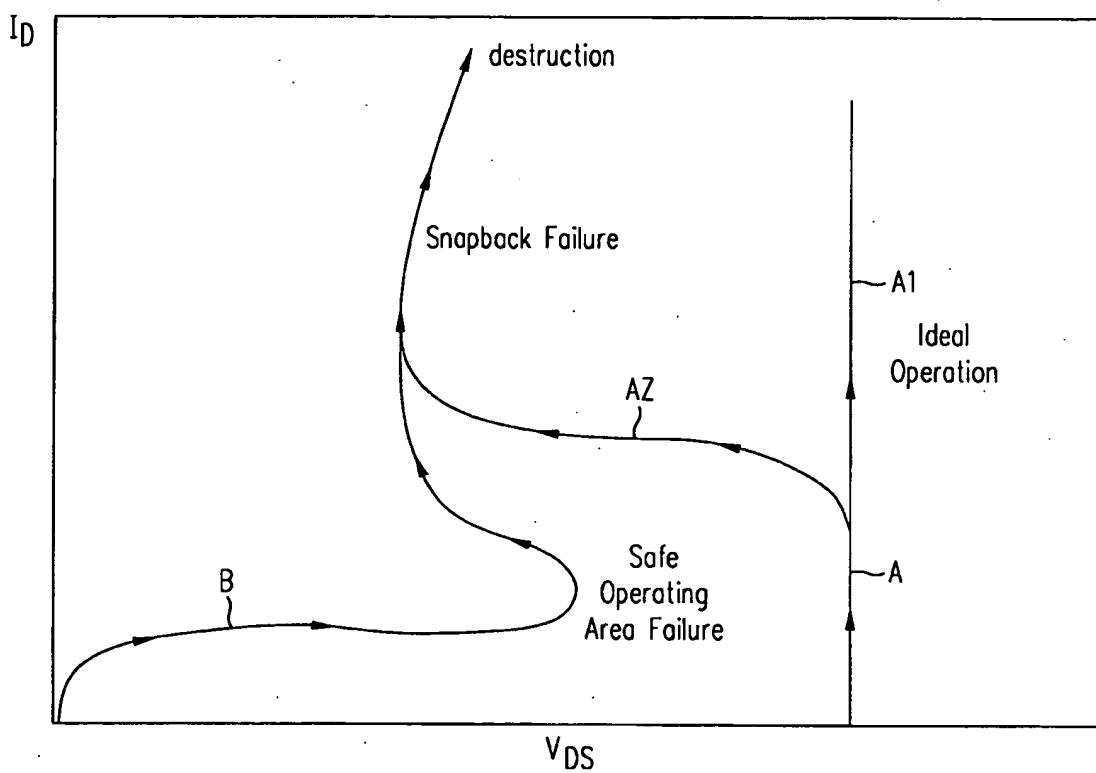


FIG. 2C
(Prior Art)

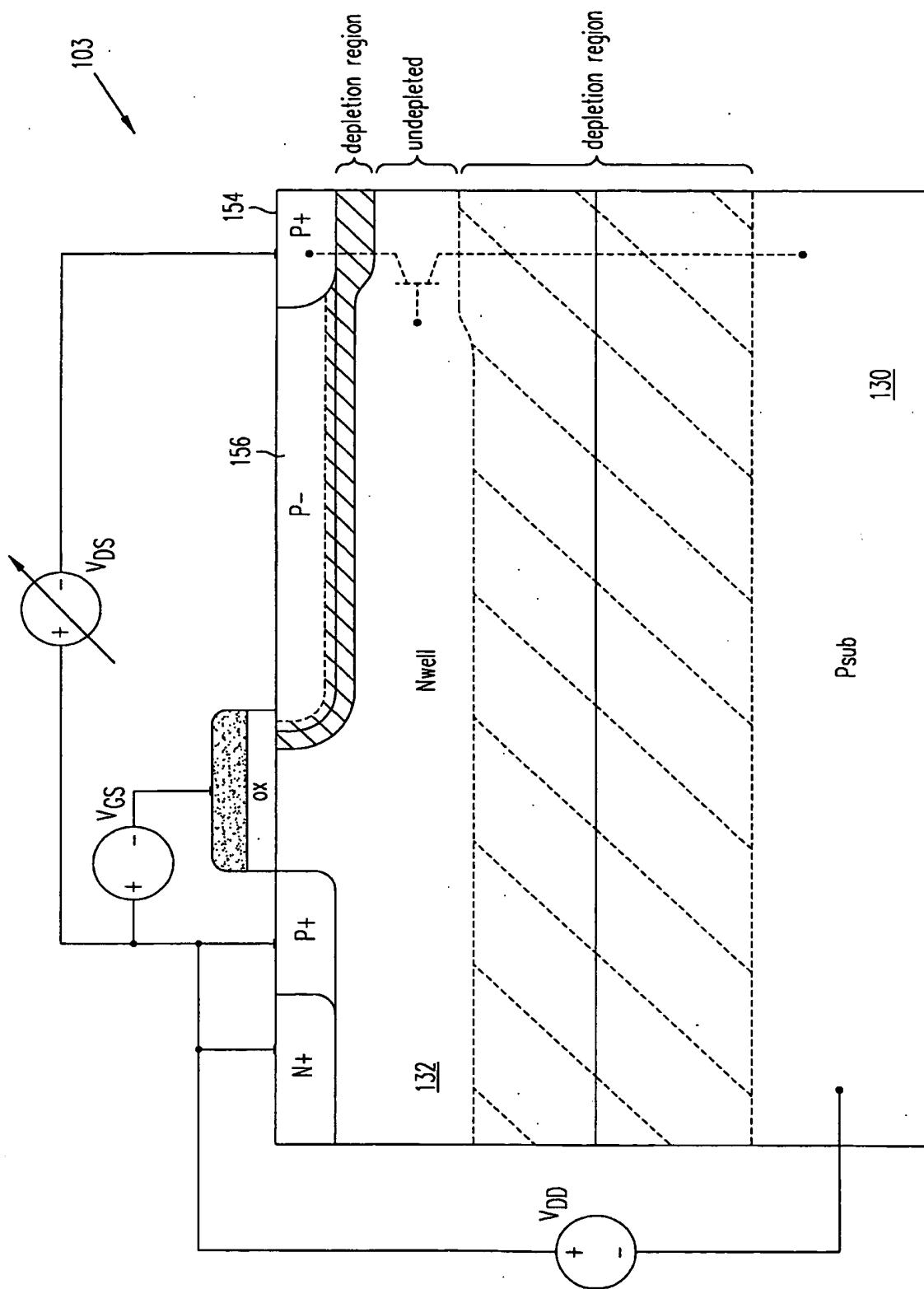


FIG. 2D (Prior Art)

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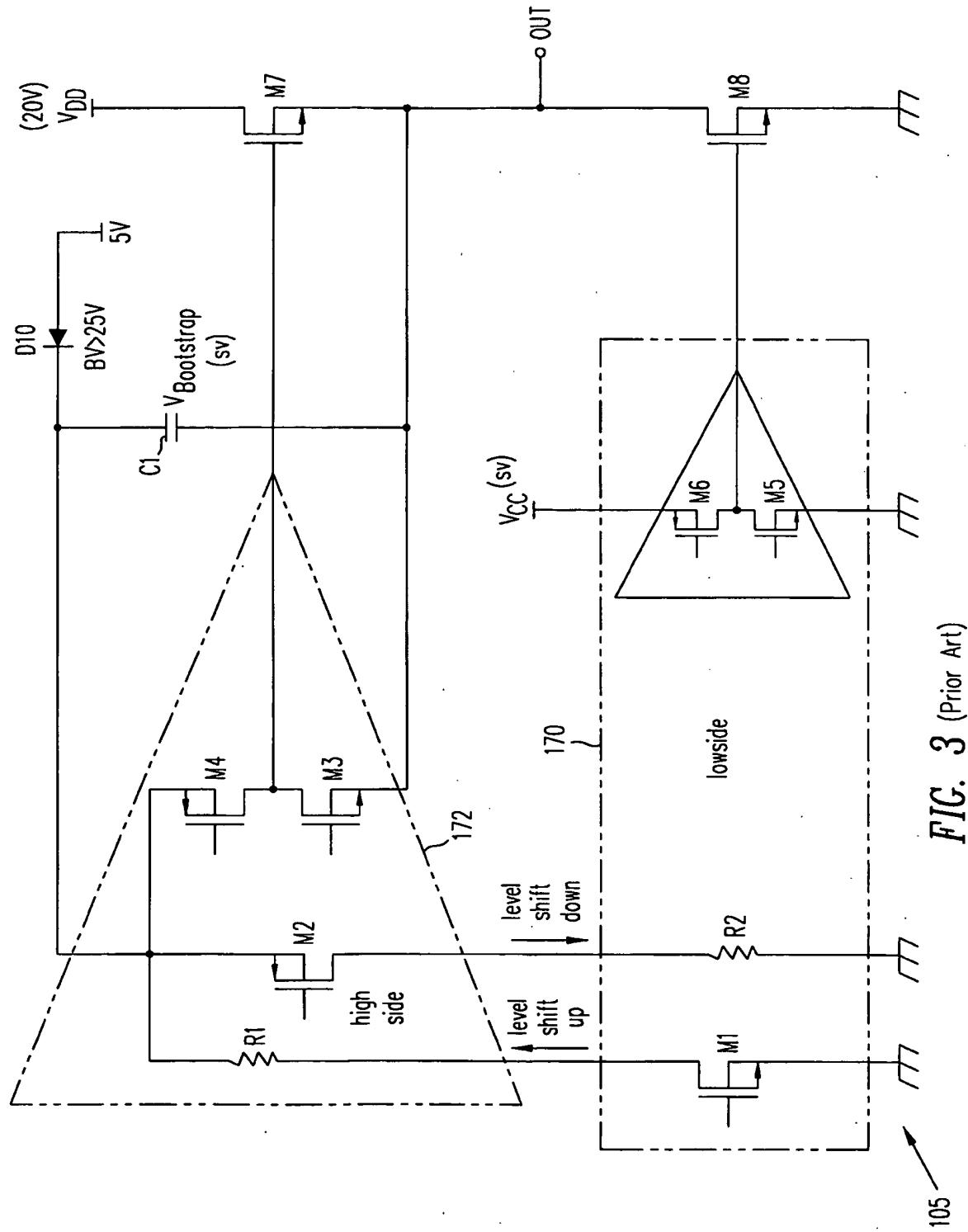


FIG. 3 (Prior Art)

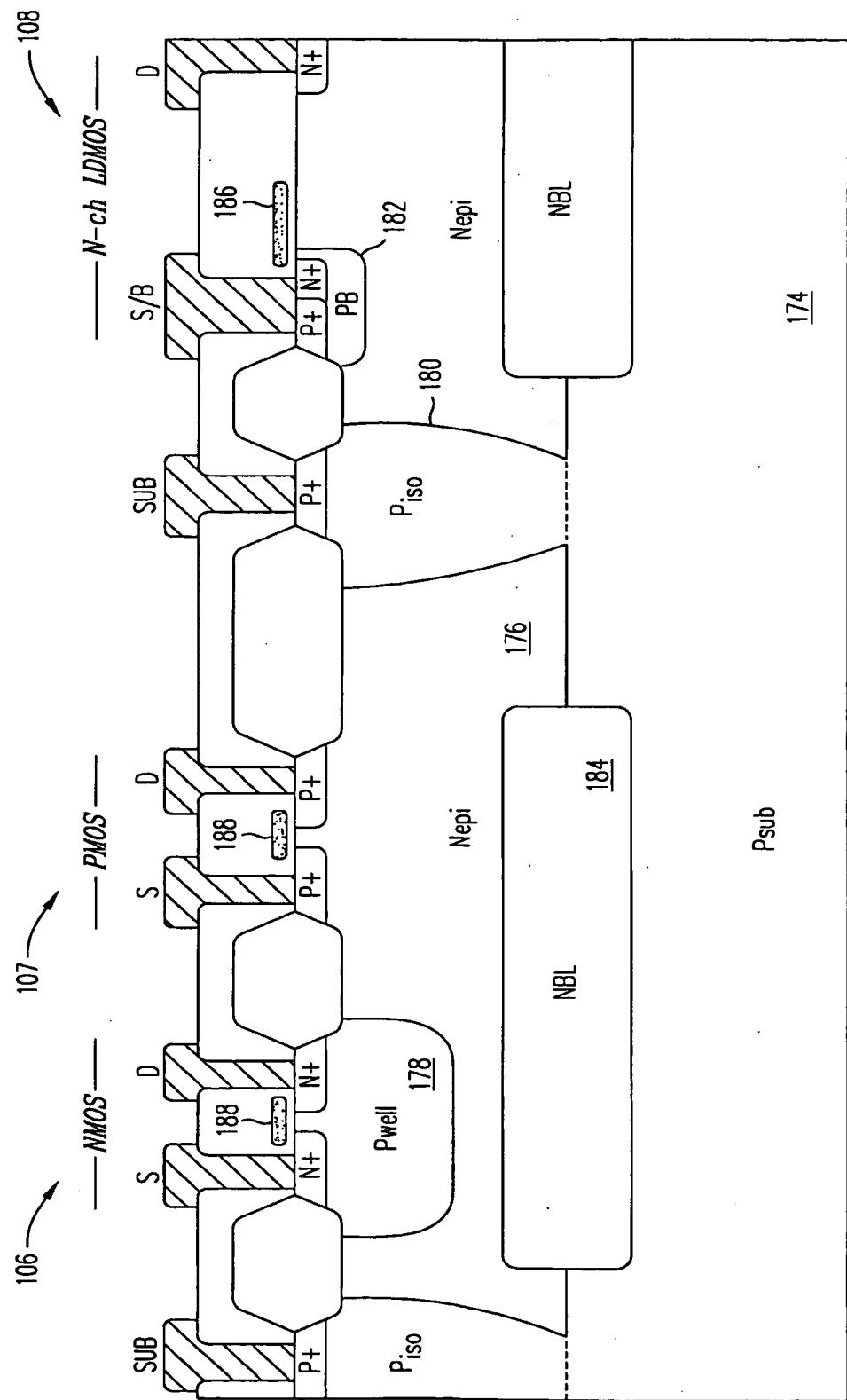


FIG. 4A
(Prior Art)

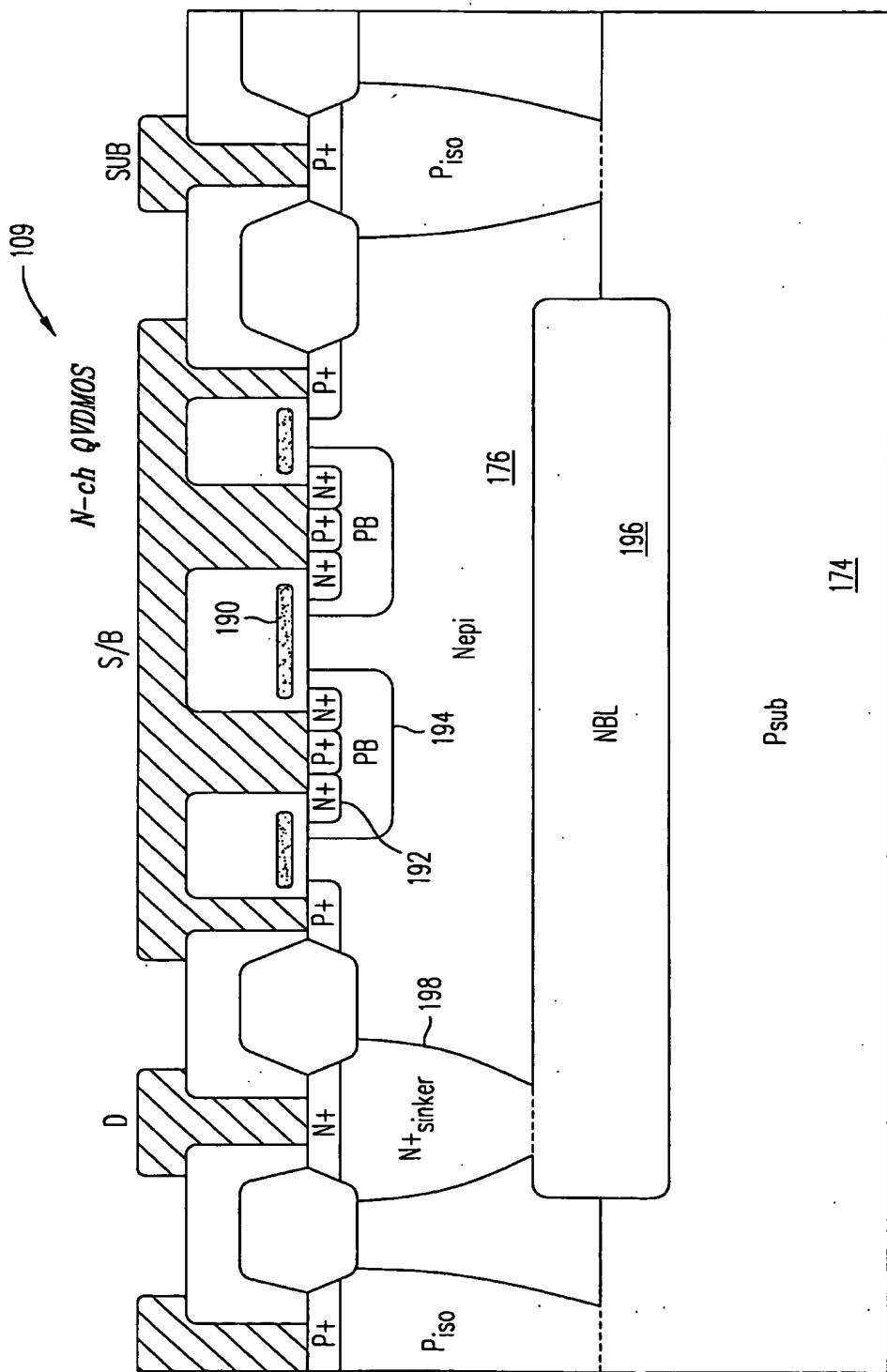


FIG. 4B
(Prior Art)

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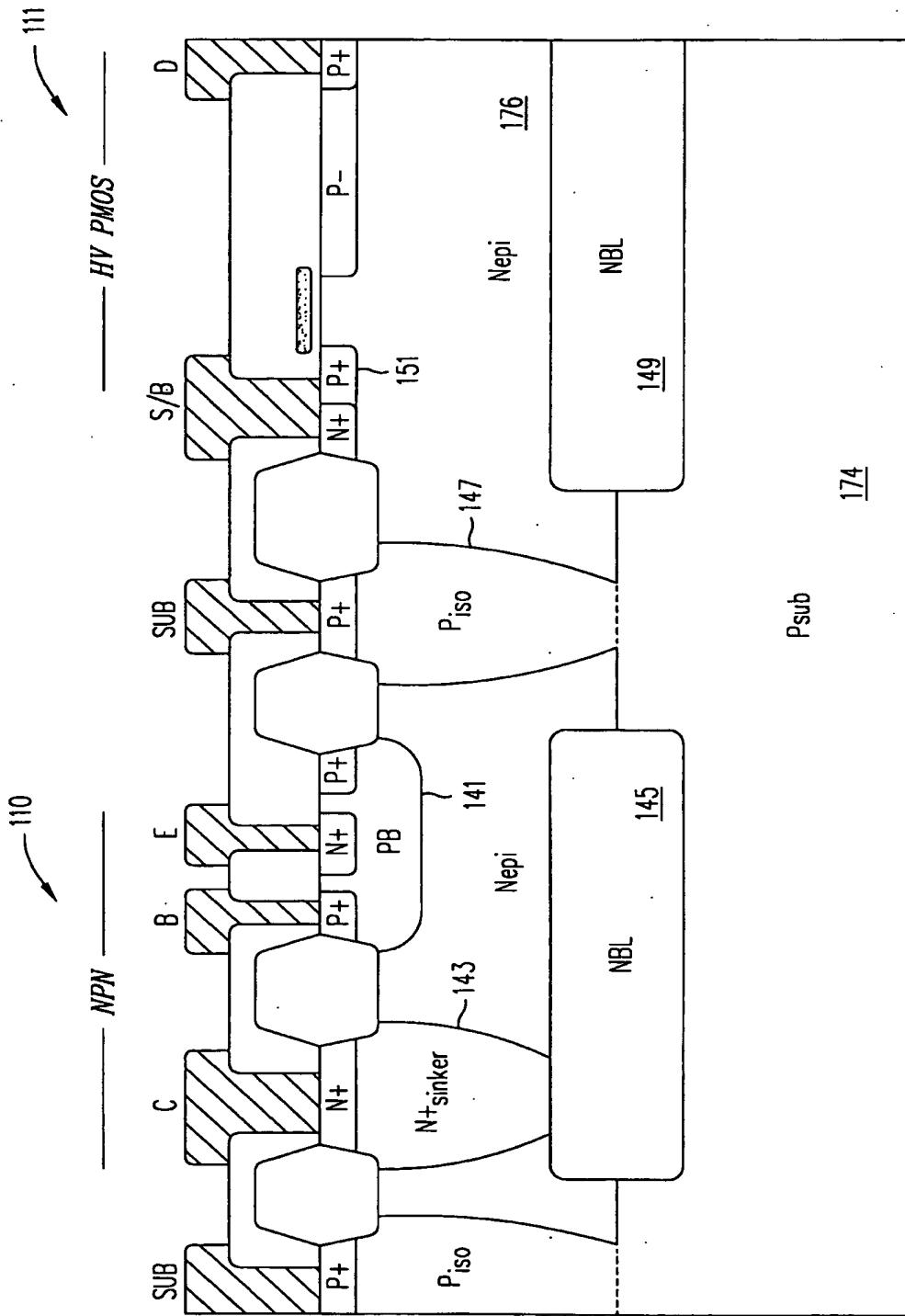


FIG. 4C
(Prior Art)

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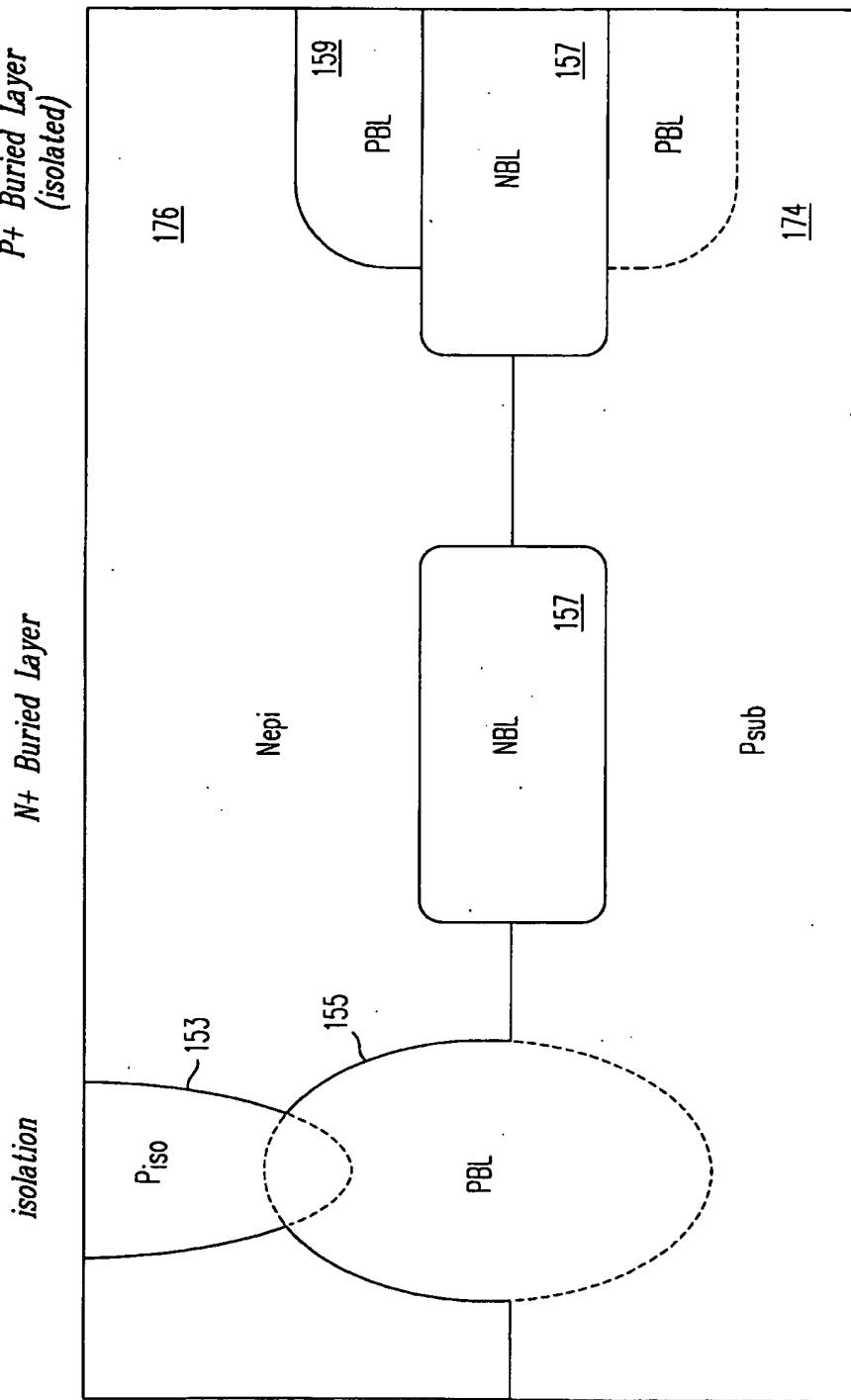


FIG. 5A
(Prior Art)

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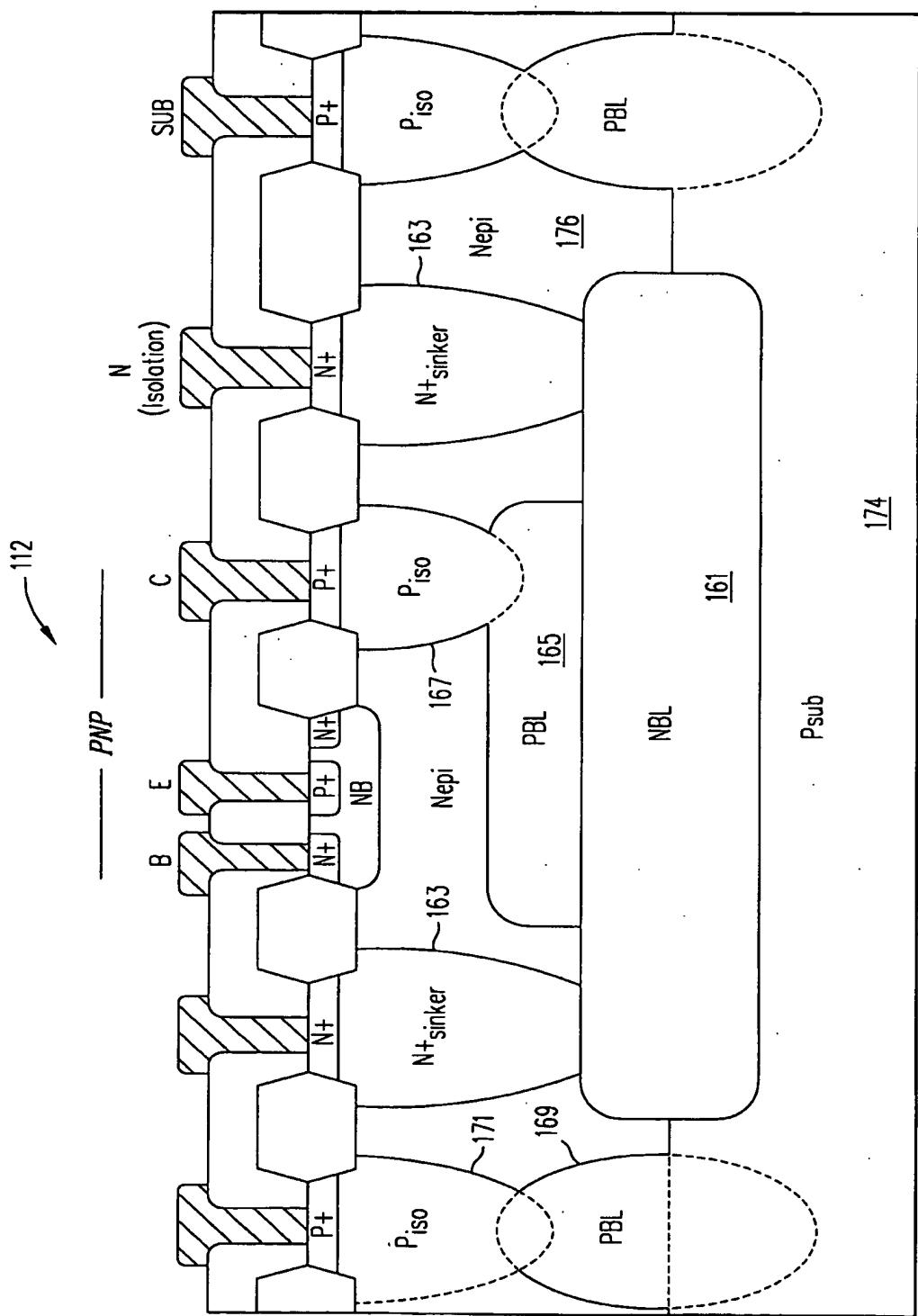


FIG. 5B (Prior Art)

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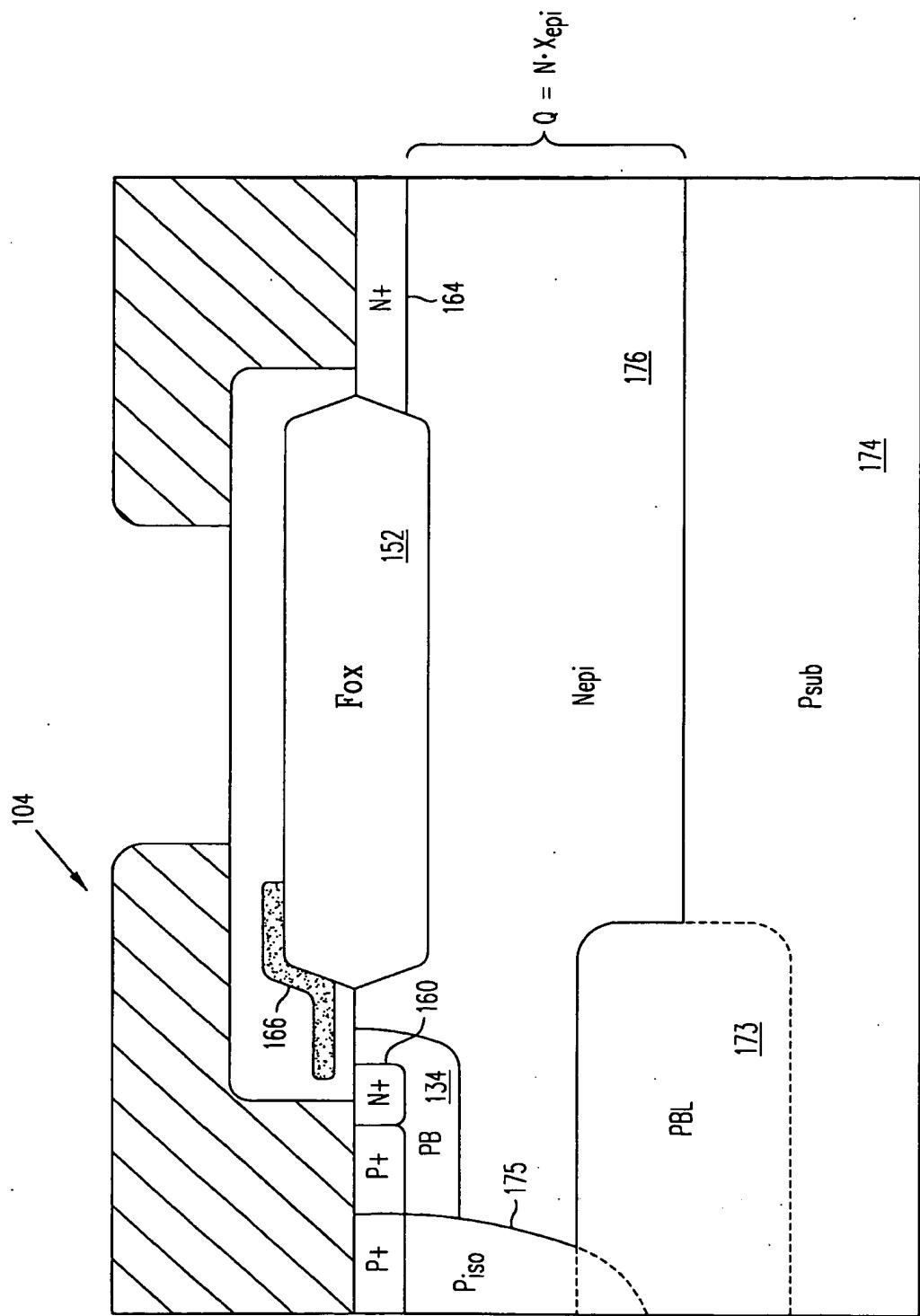


FIG. 5C
(Prior Art)

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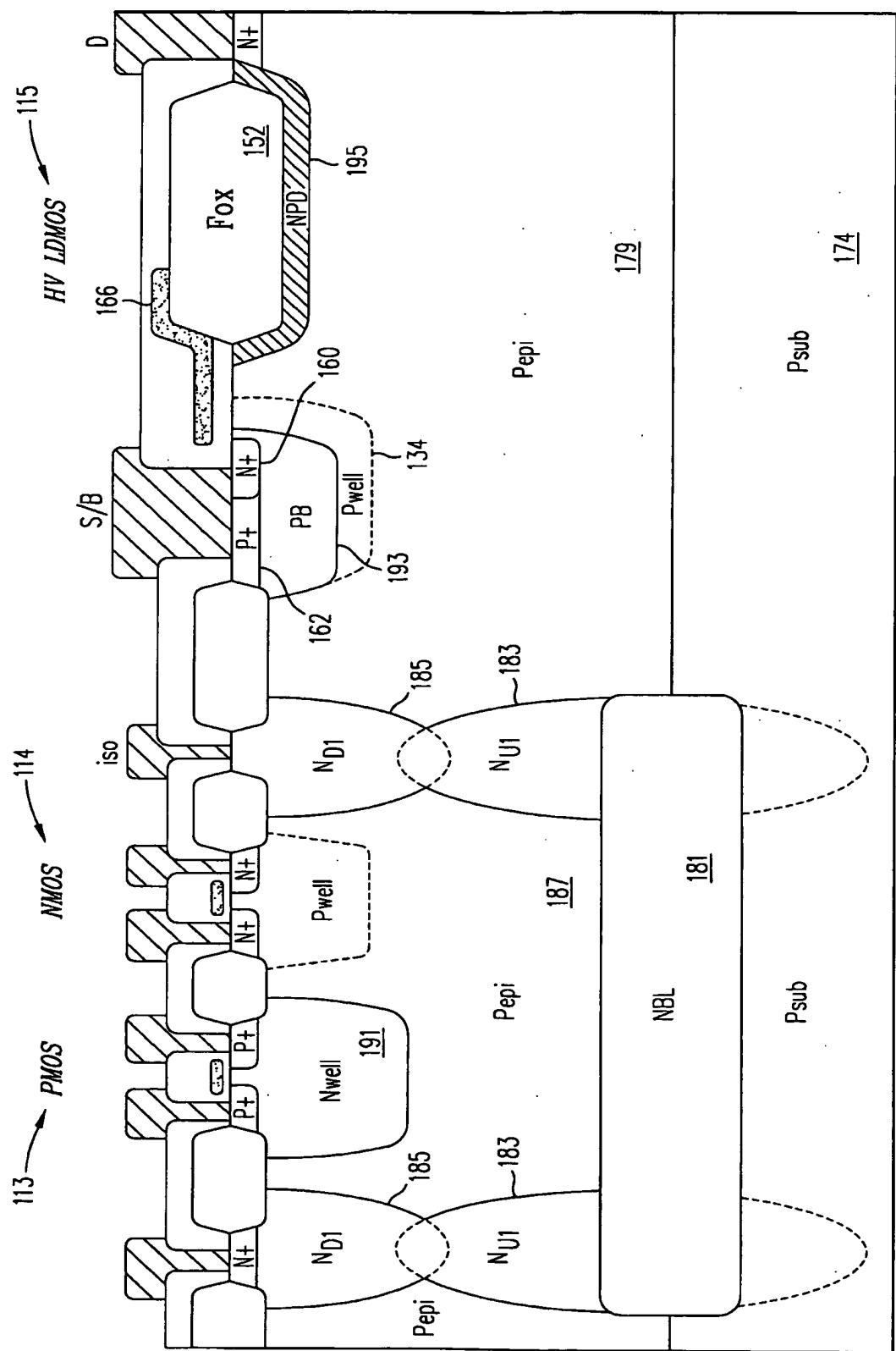


FIG. 6A (Prior Art)

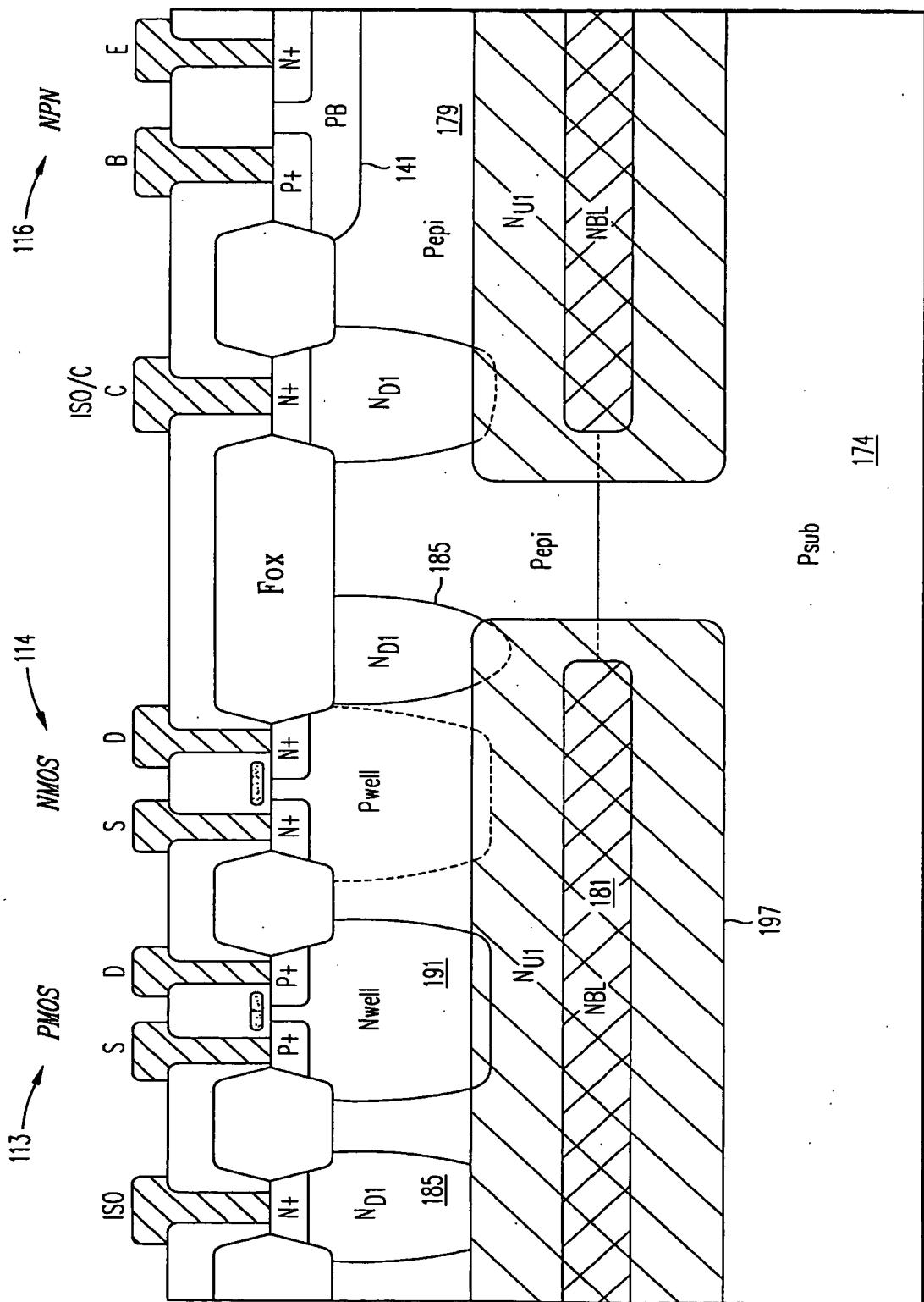


FIG. 6B (Prior Art)

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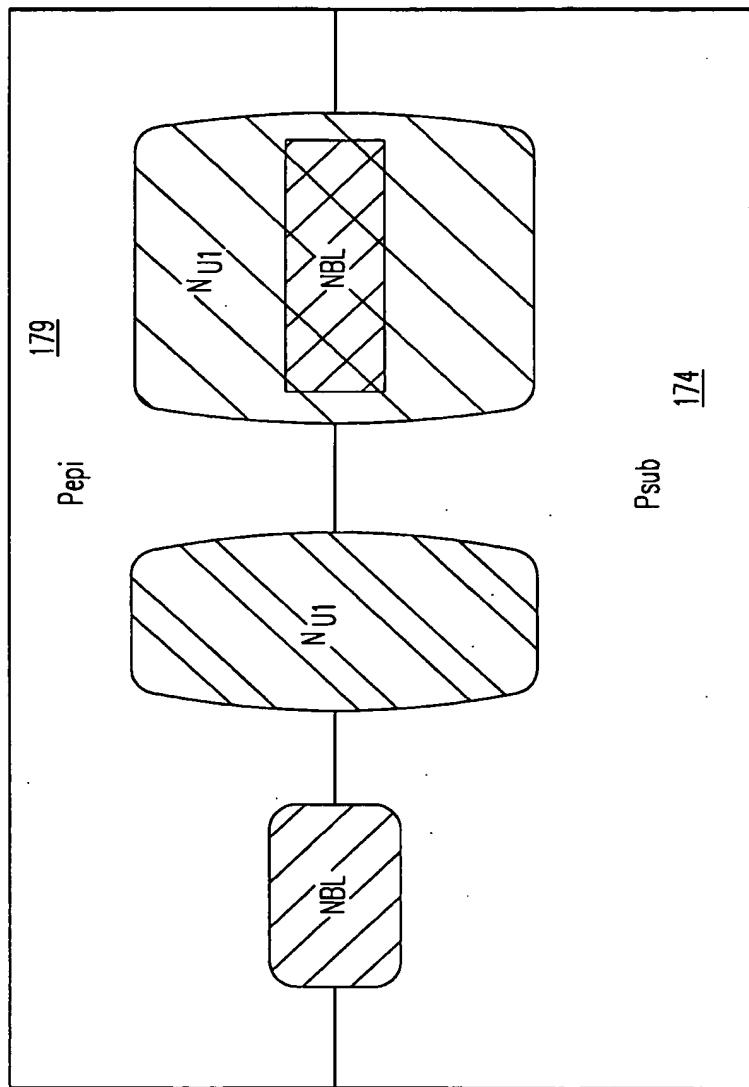


FIG. 6C
(Prior Art)

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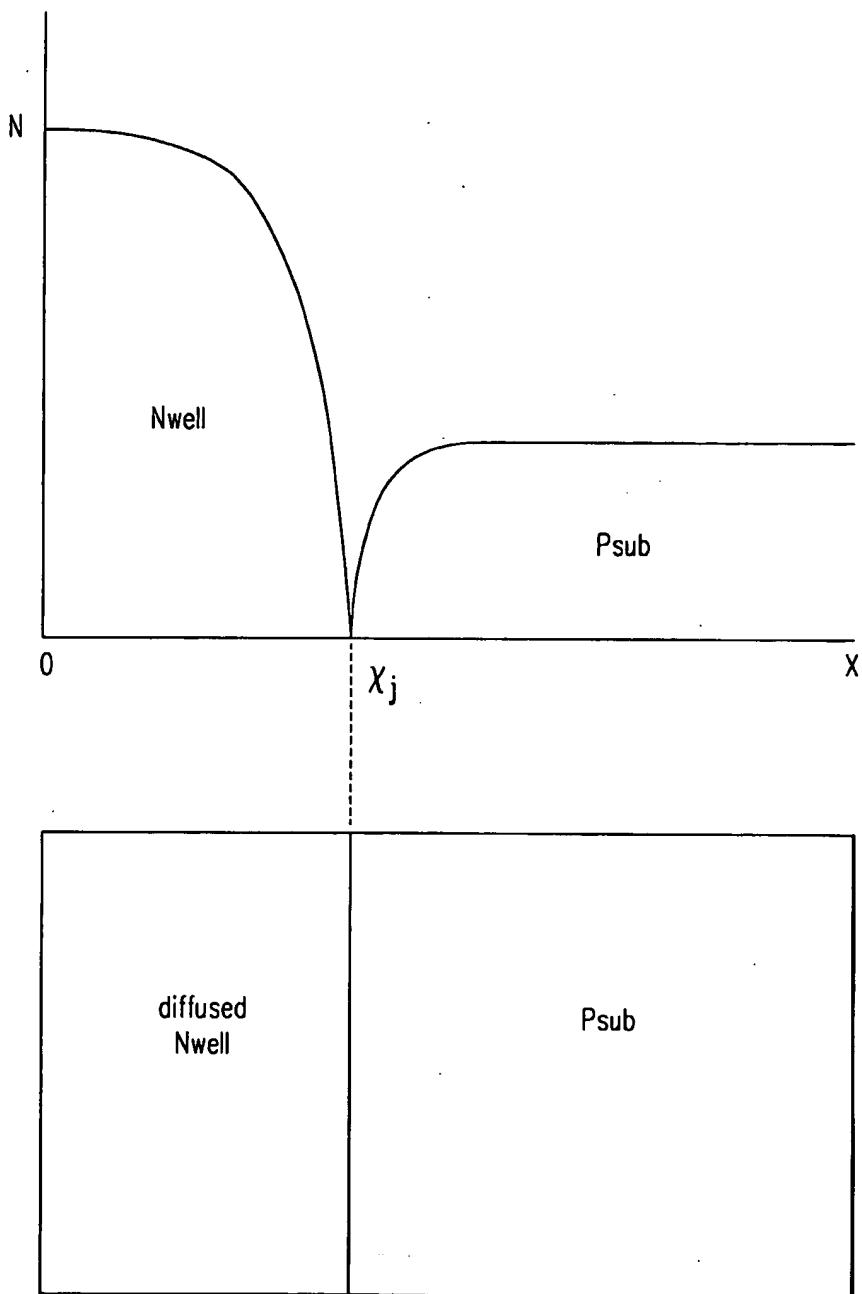


FIG. 7A
(Prior Art)

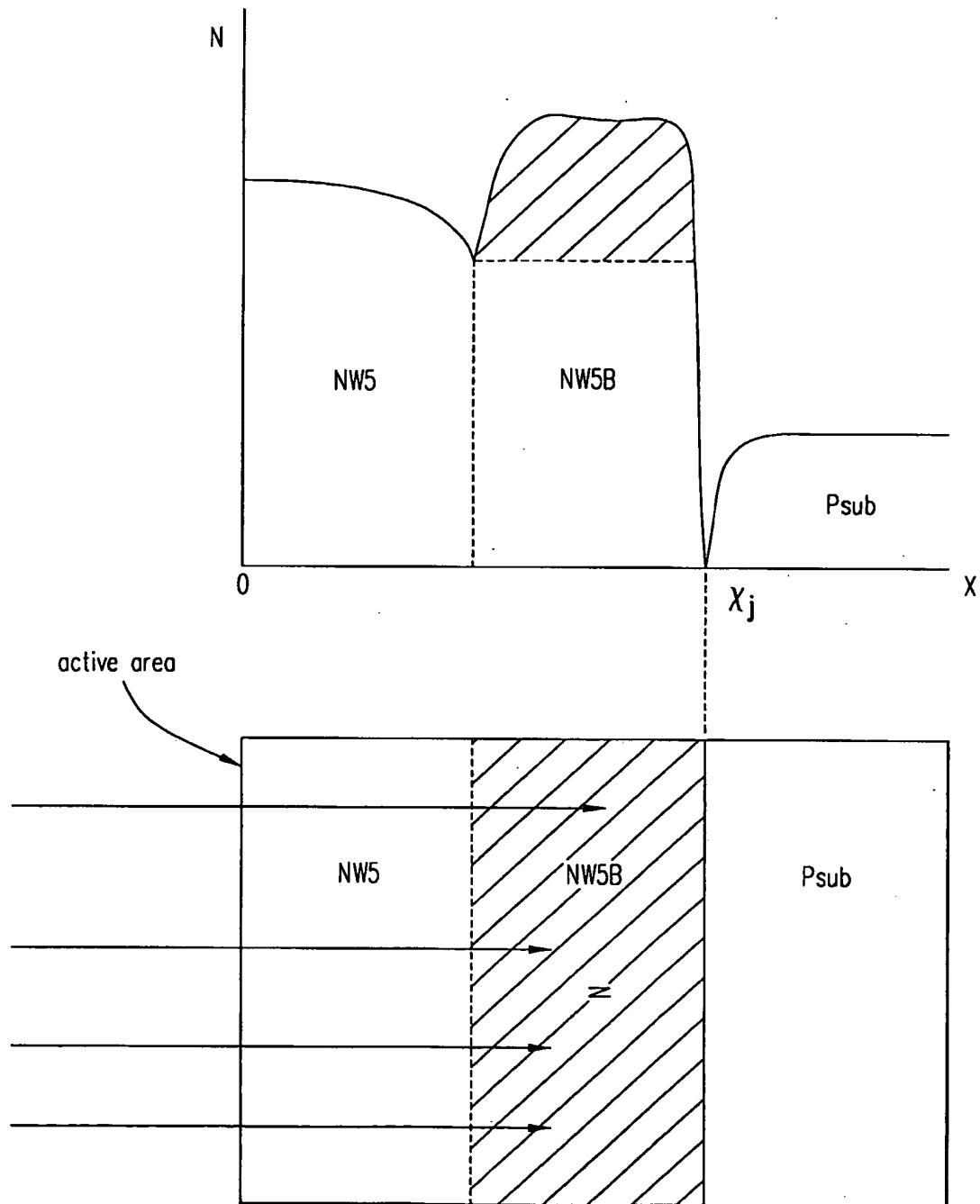


FIG. 7B

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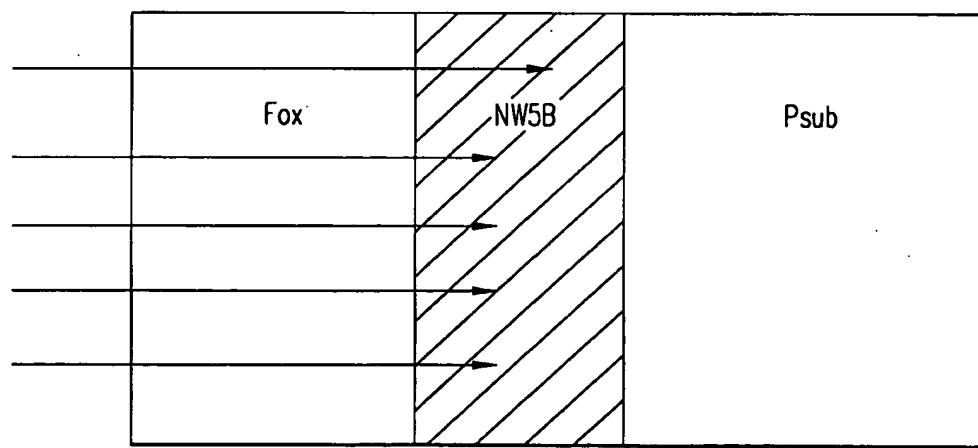
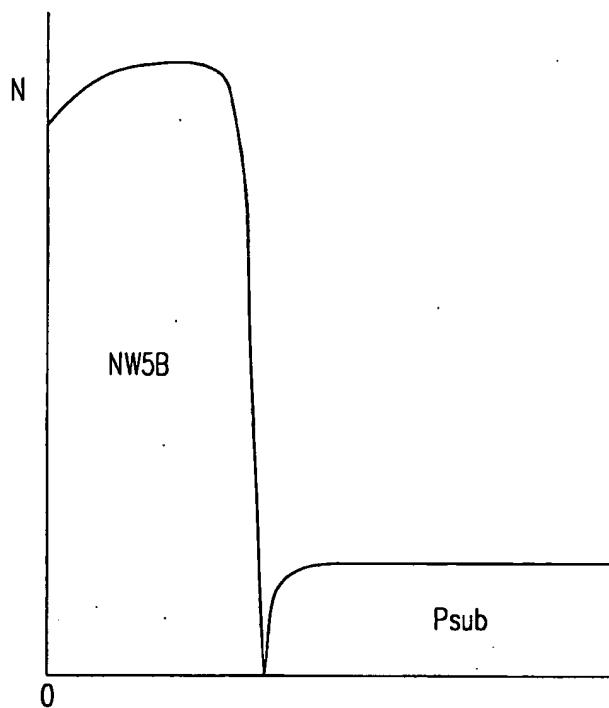


FIG. 7C

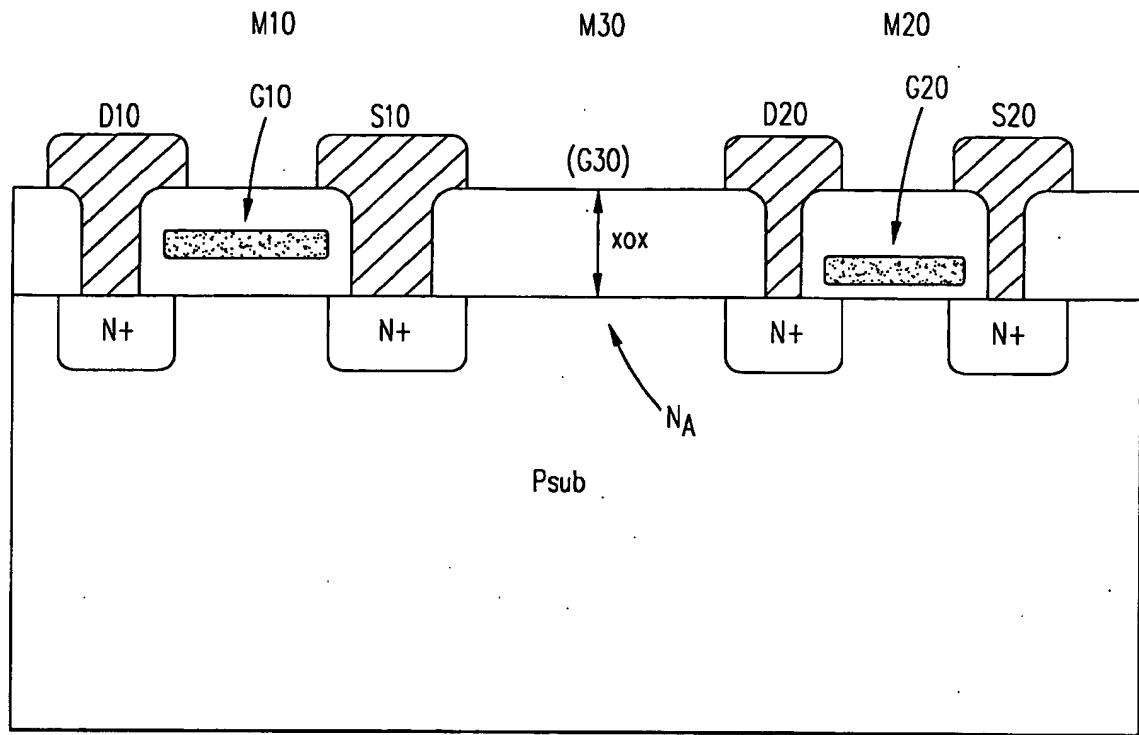


FIG. 8A

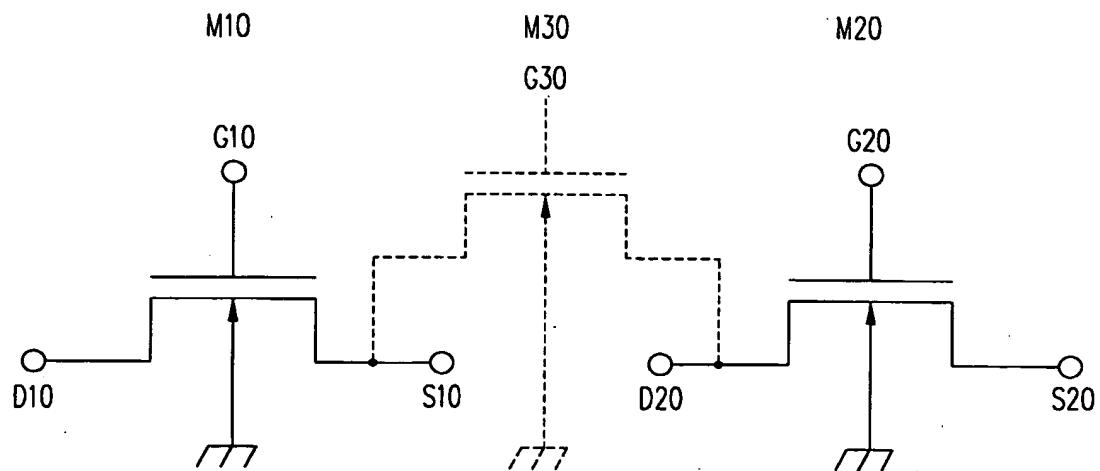


FIG. 8B

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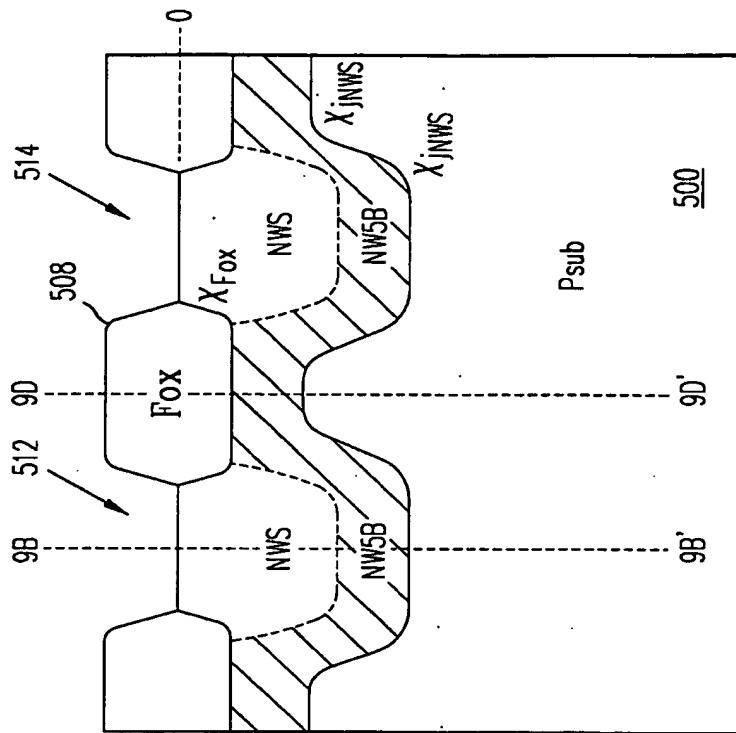


FIG. 9B

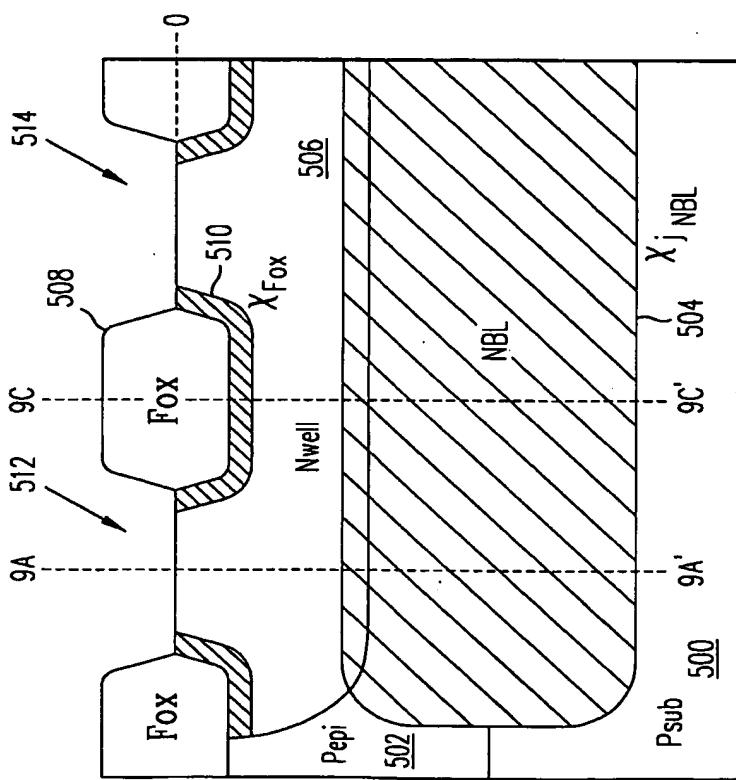


FIG. 9A
(Prior Art)

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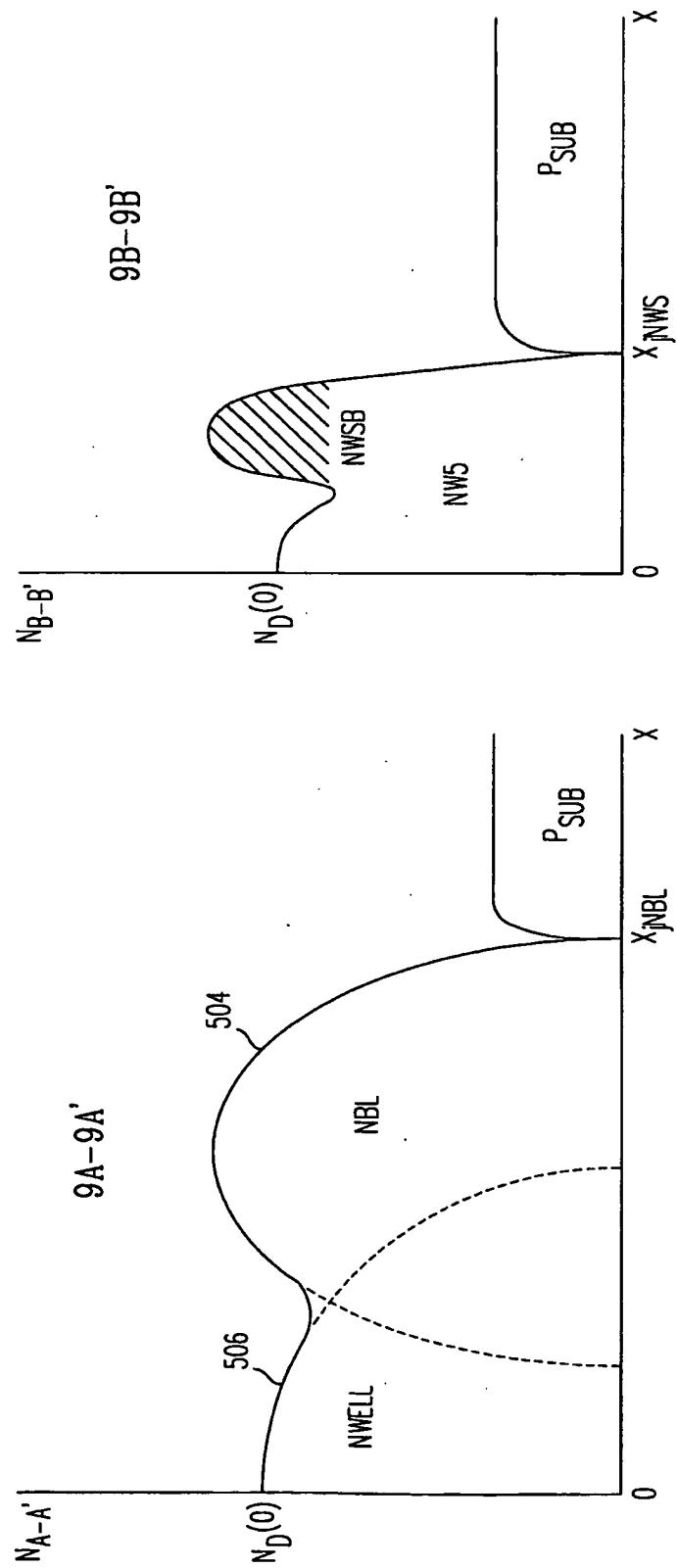


FIG. 9D
(Prior Art)

FIG. 9C
(Prior Art)

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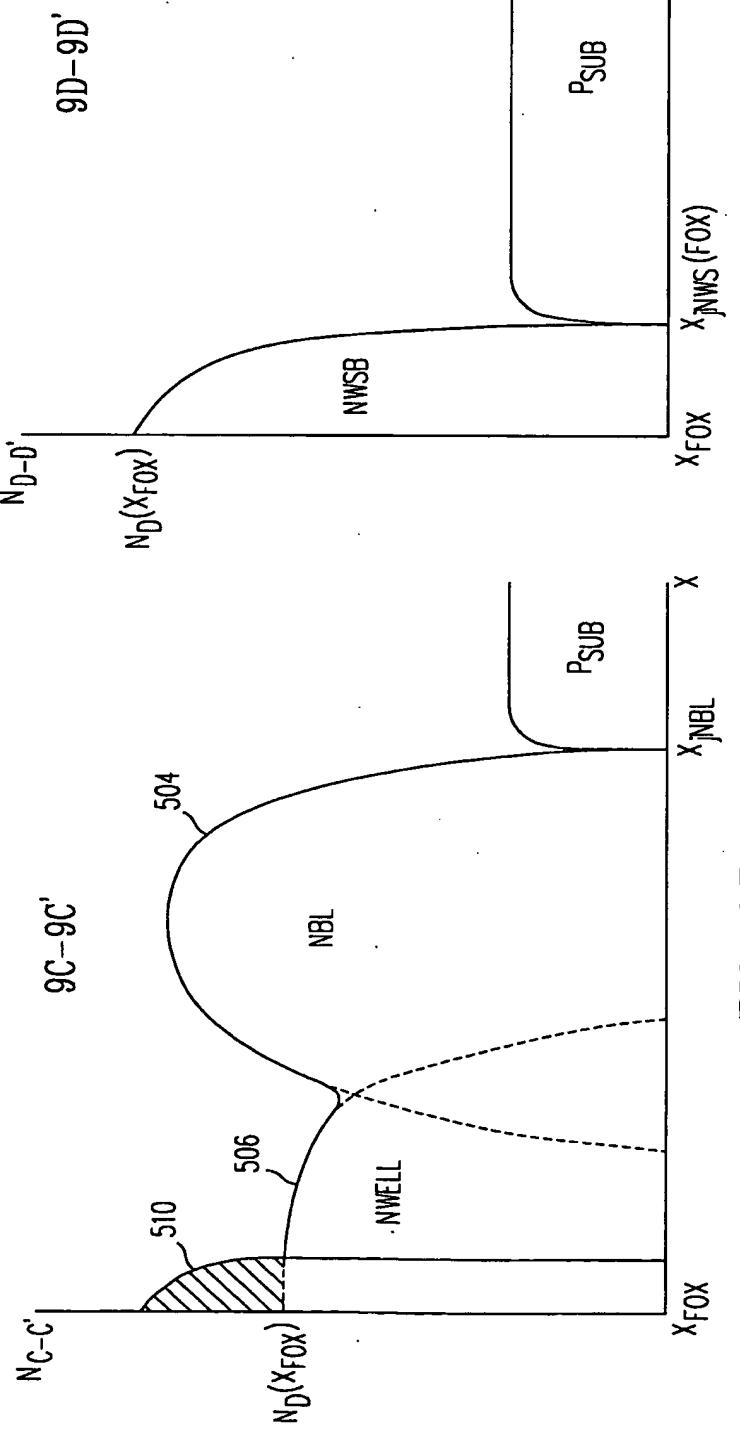


FIG. 9F
(Prior Art)

FIG. 9E
(Prior Art)

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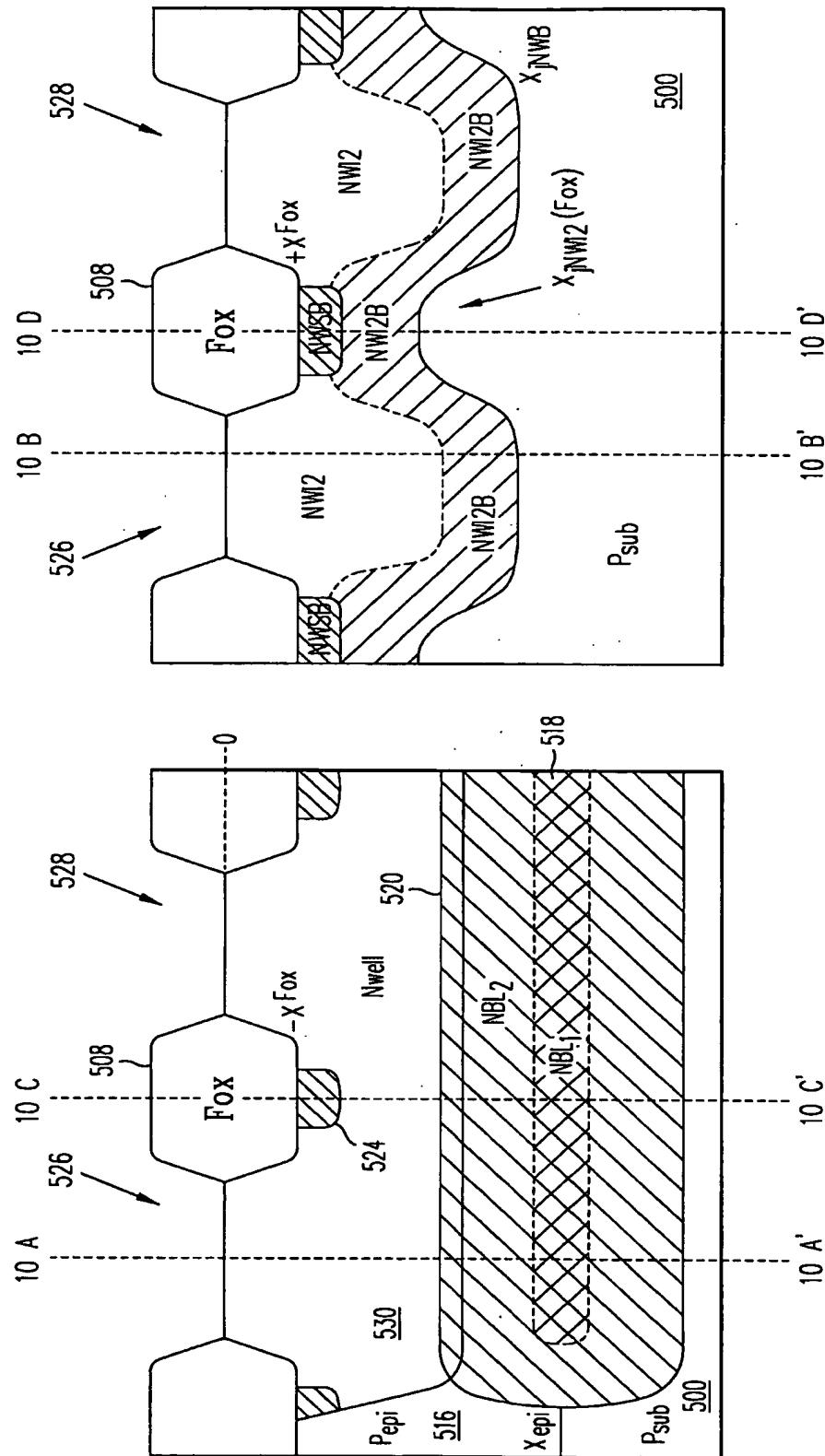


FIG. 10A
(Prior Art)

FIG. 10B

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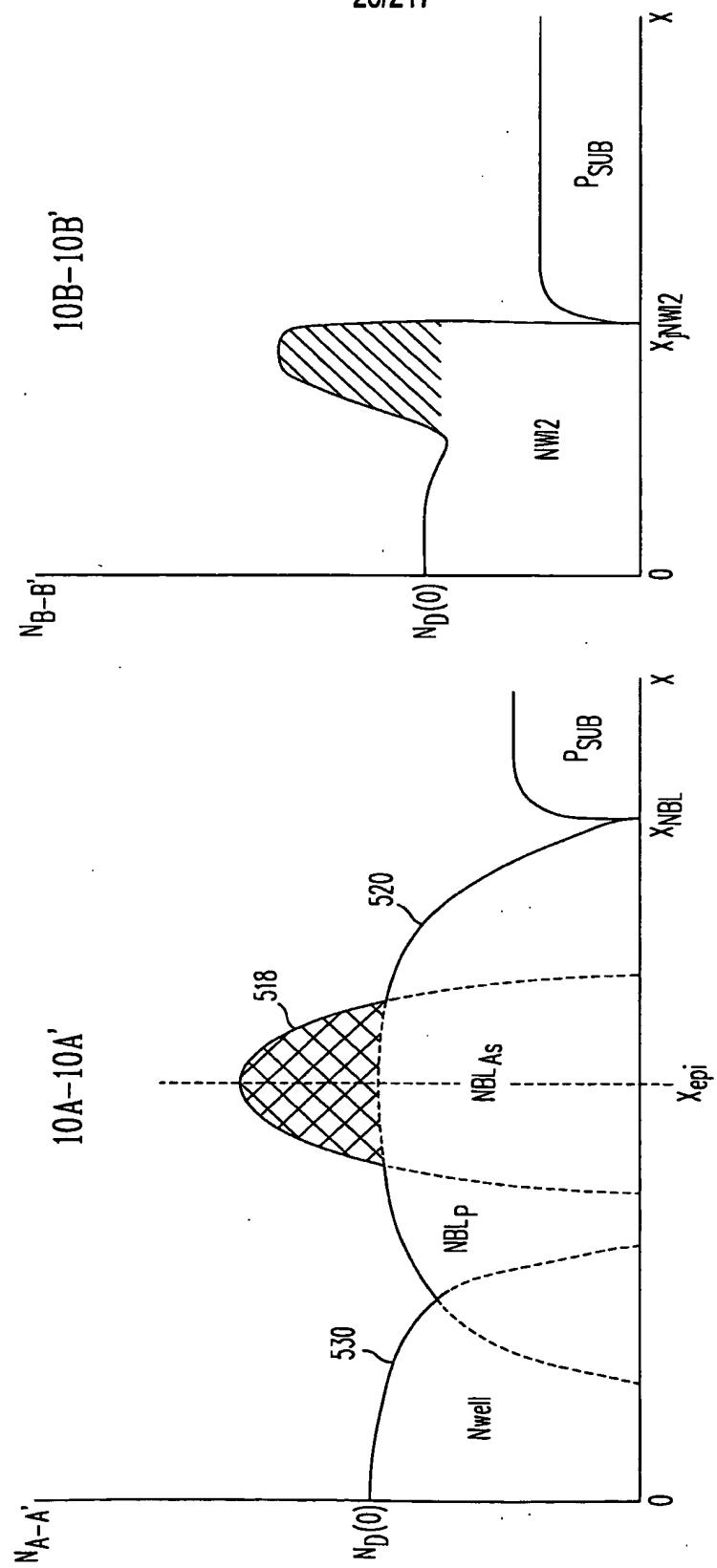


FIG. 10C
(Prior Art)

FIG. 10D

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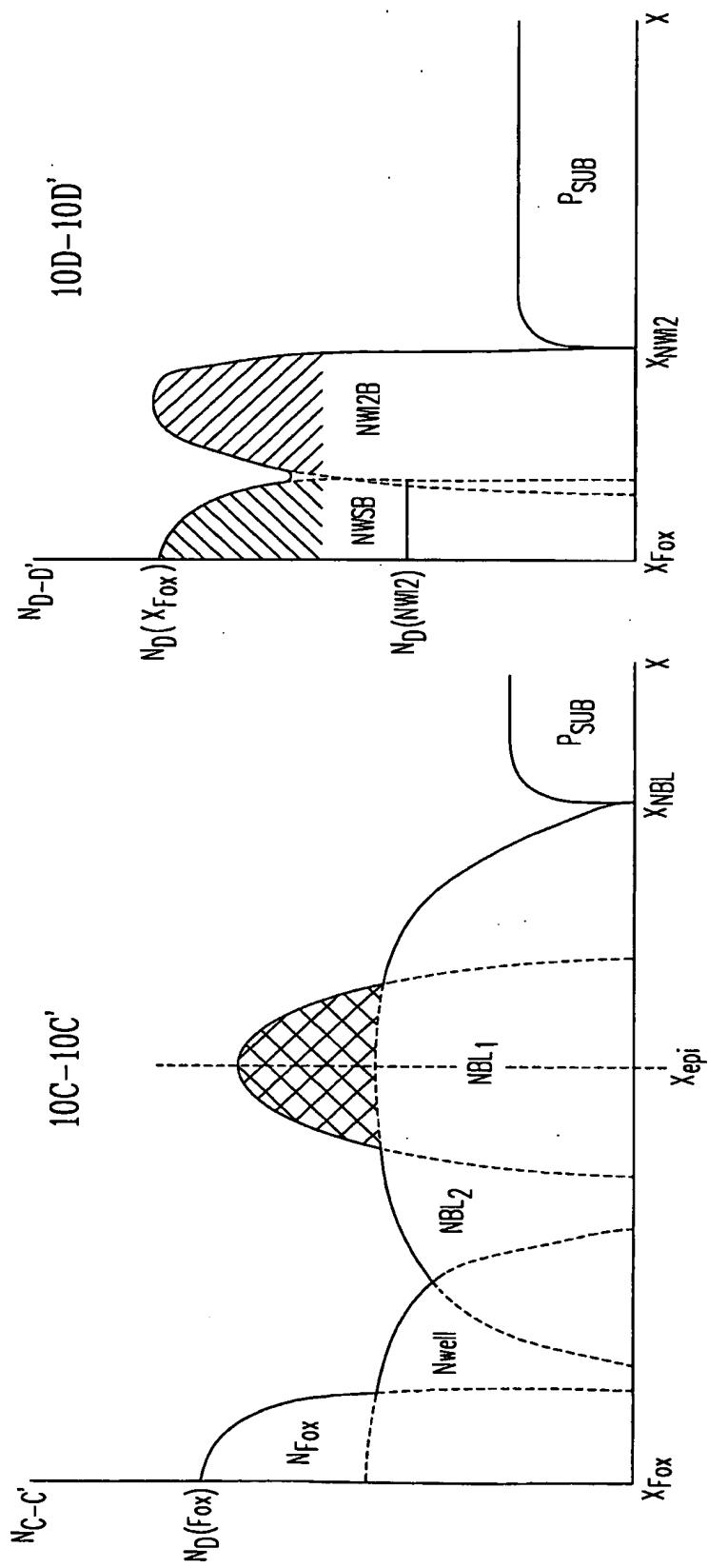


FIG. 10E
(Prior Art)

FIG. 10F

FIG. 10I

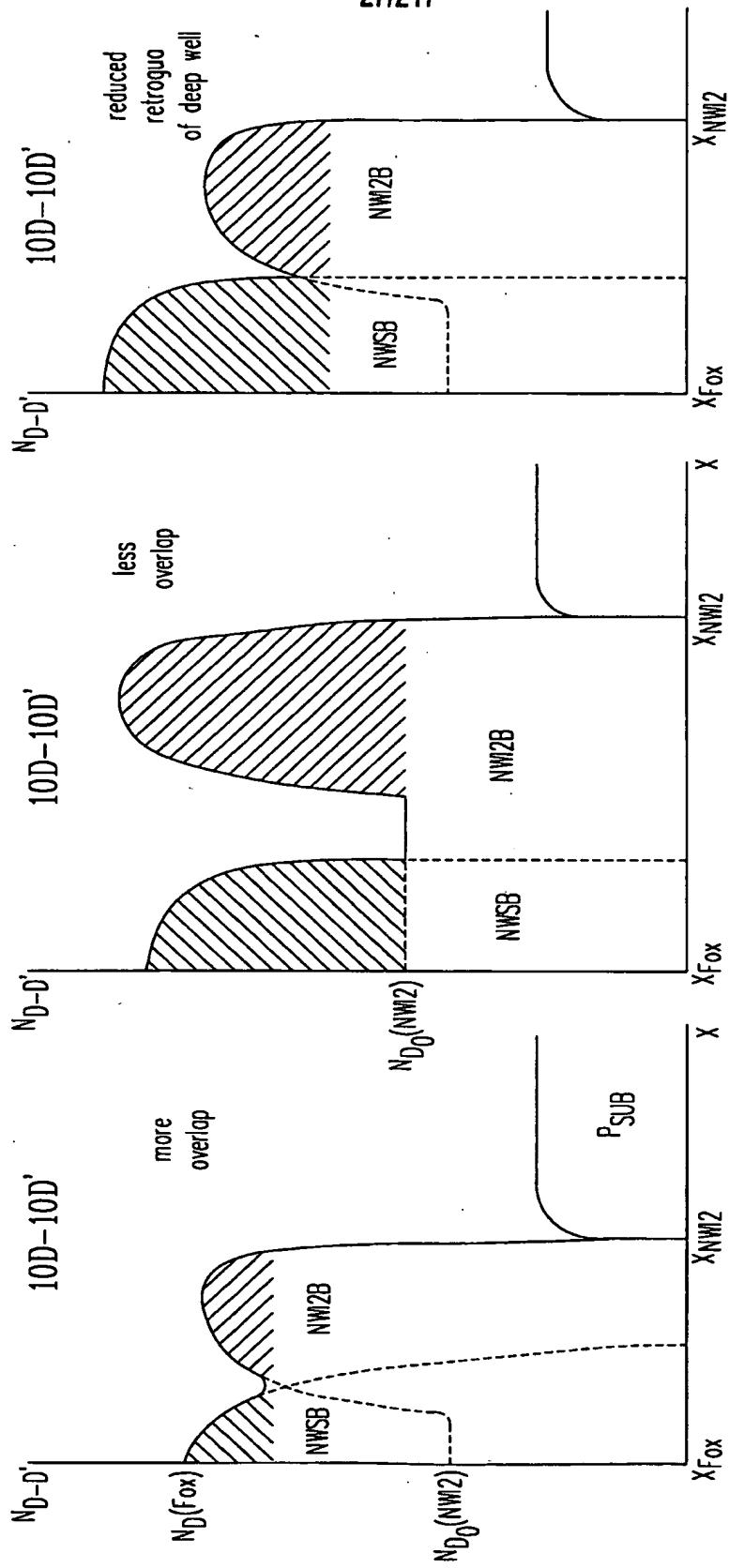


FIG. 10H

FIG. 10G

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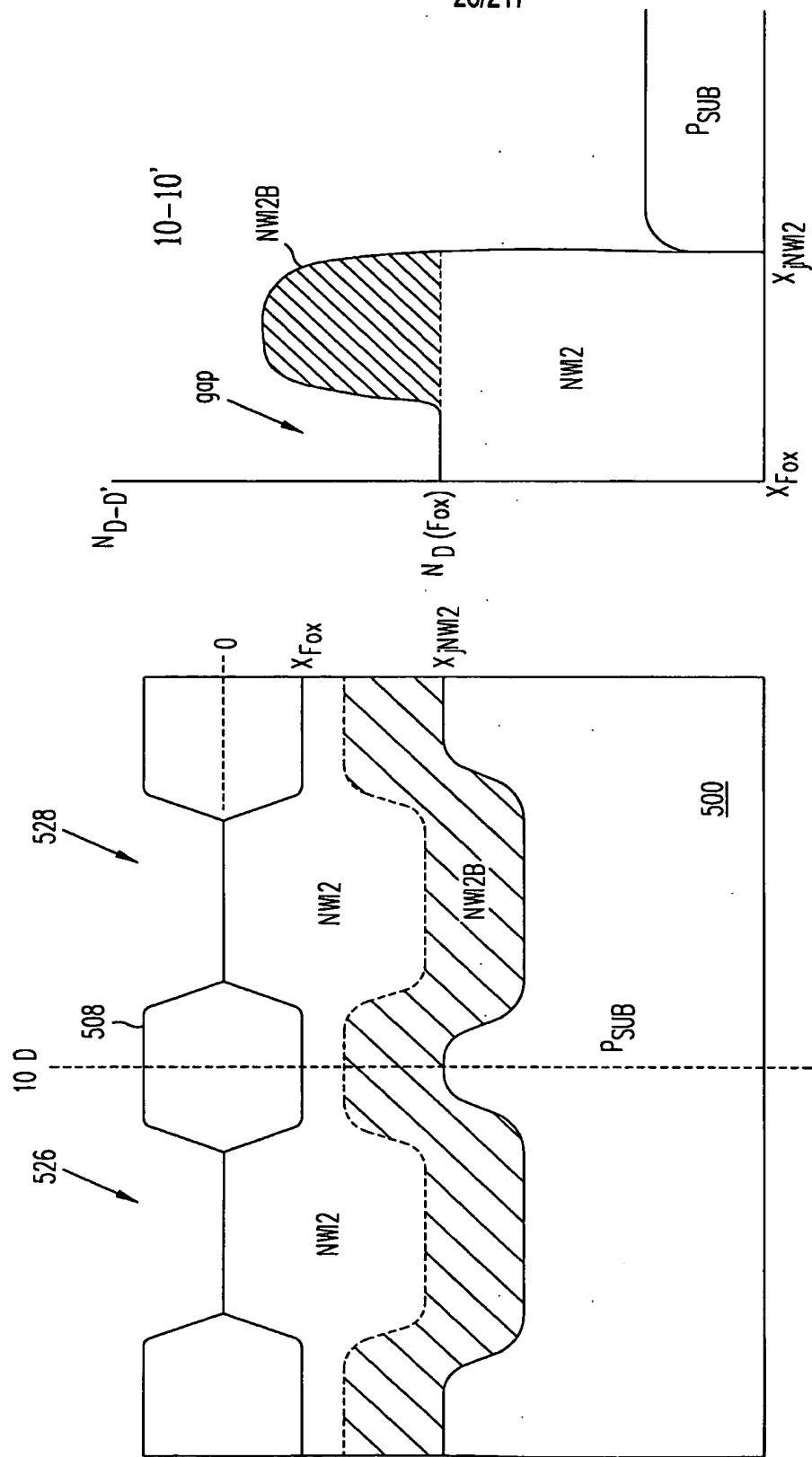
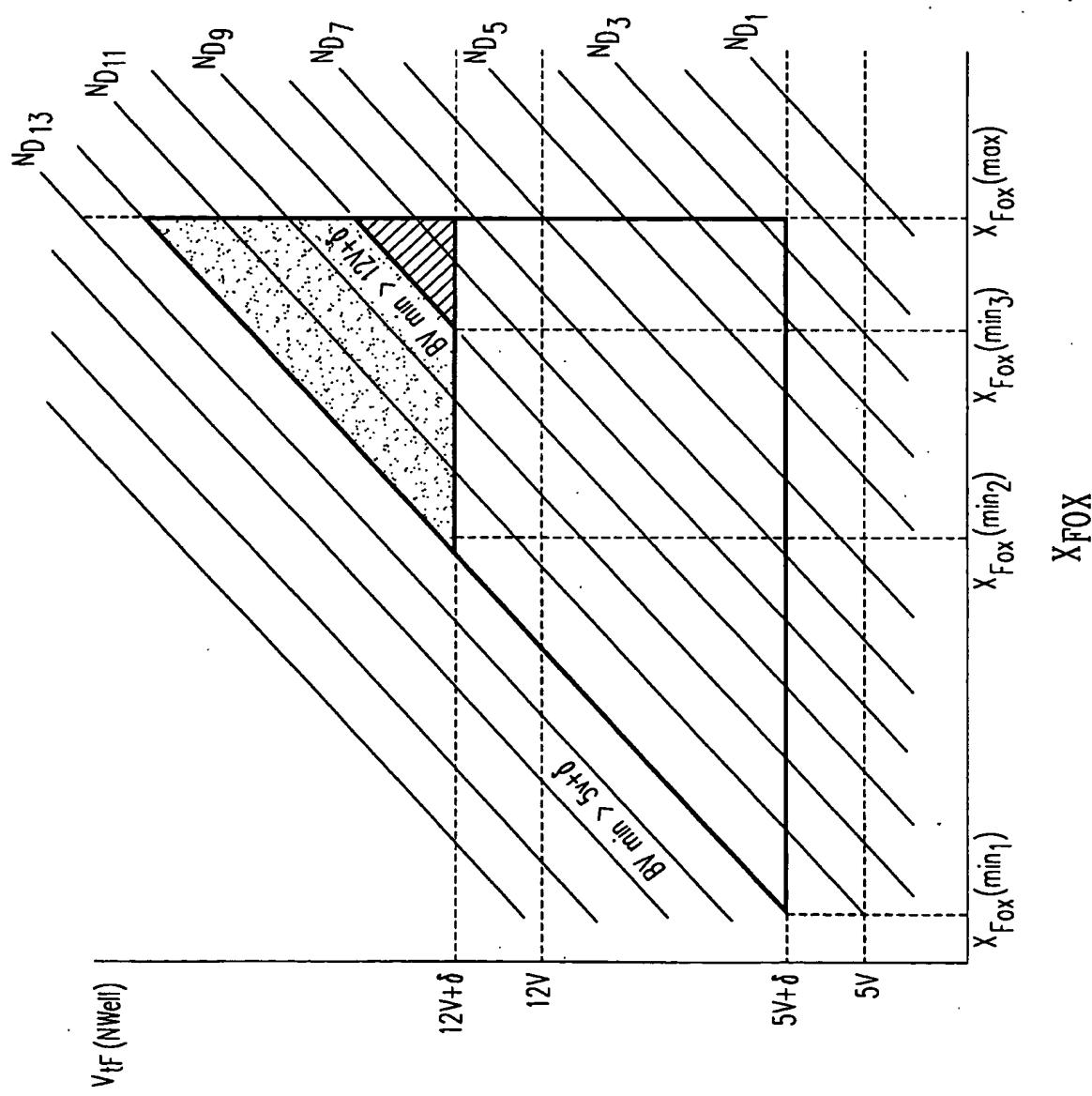


FIG. 10K

FIG. 10J



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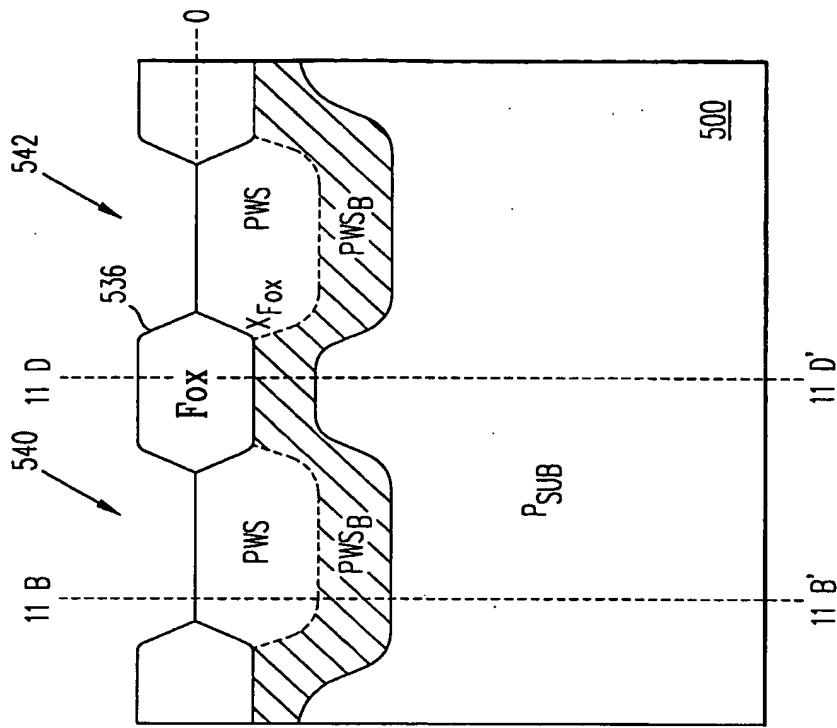


FIG. 11B

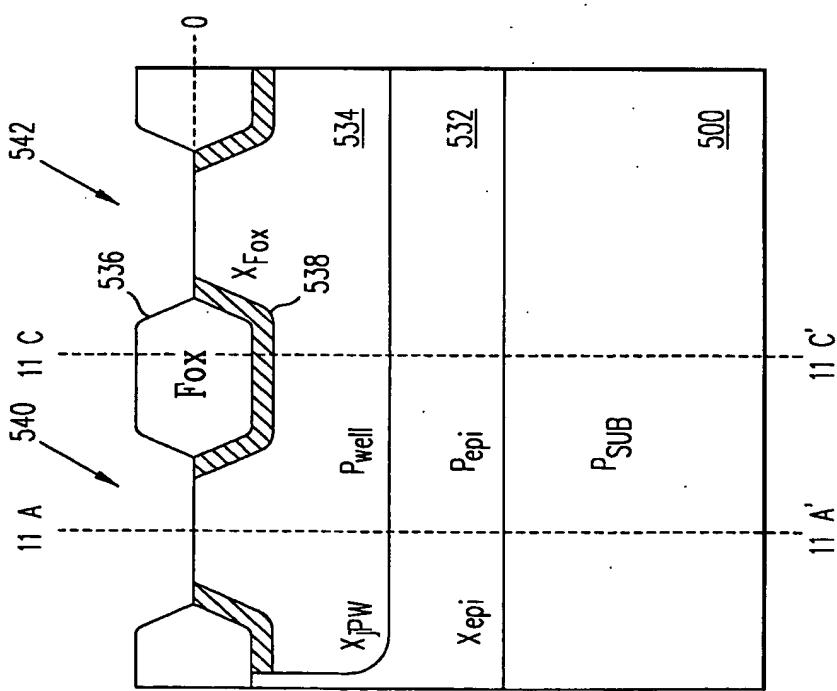


FIG. 11A

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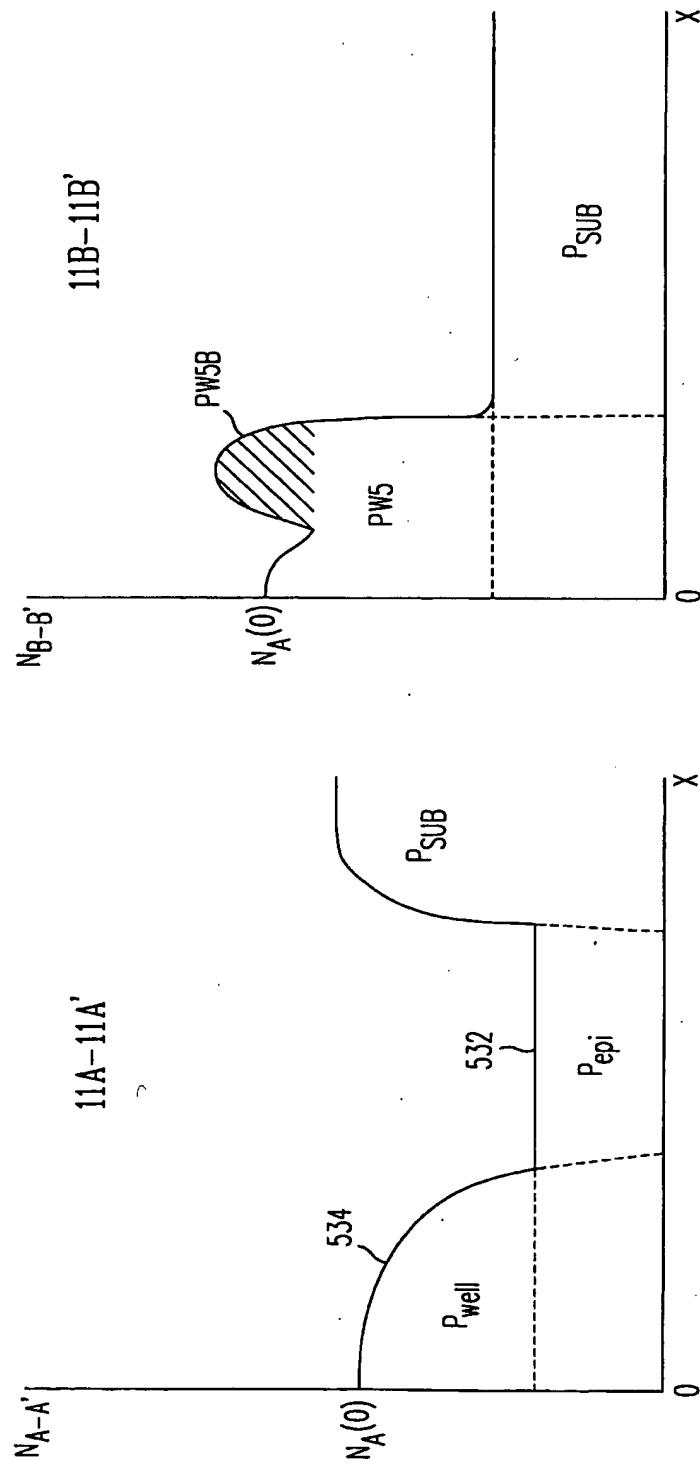


FIG. 11C

FIG. 11D

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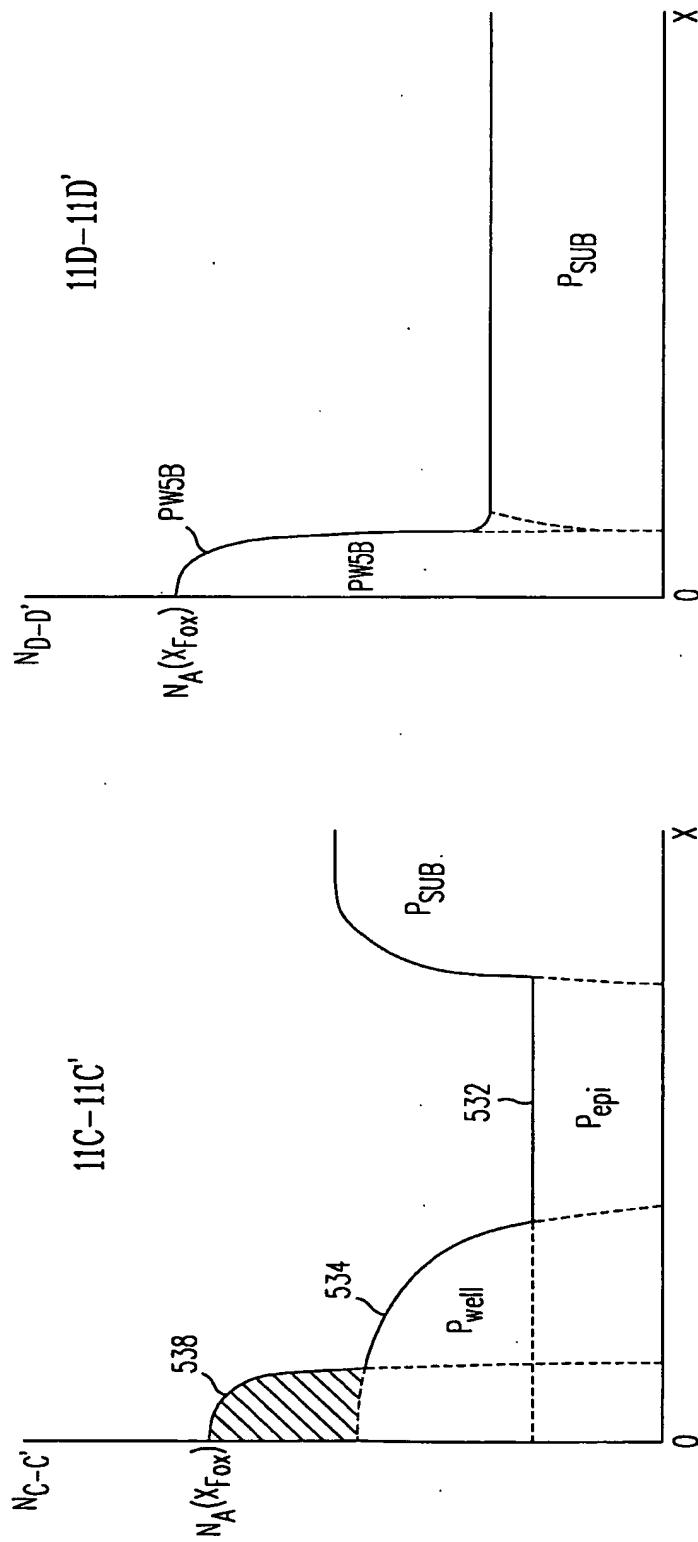


FIG. 11F

FIG. 11E

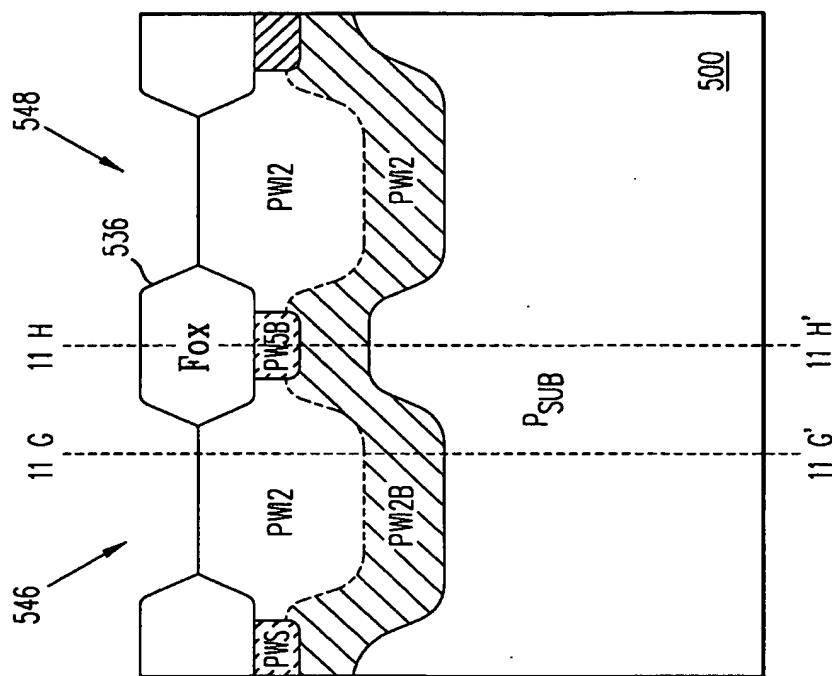


FIG. 11H

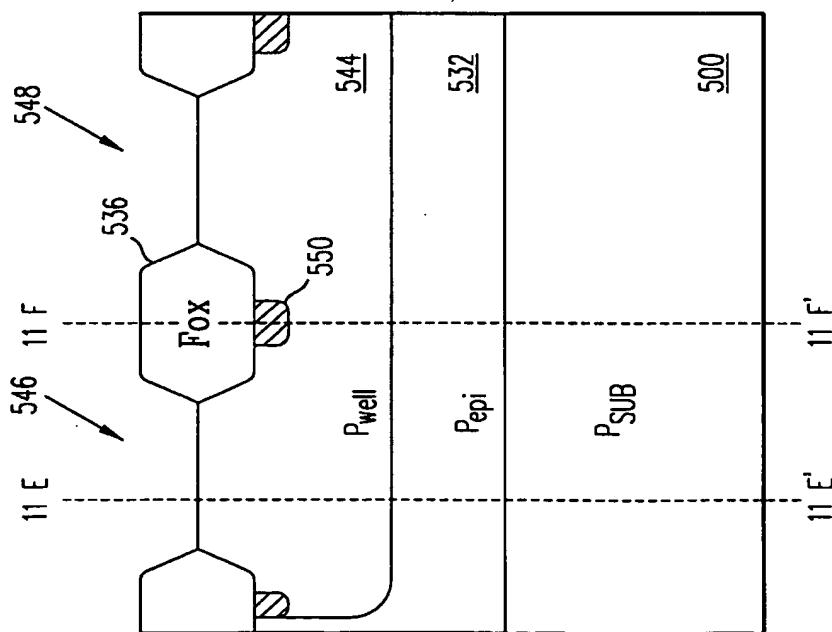


FIG. 11G

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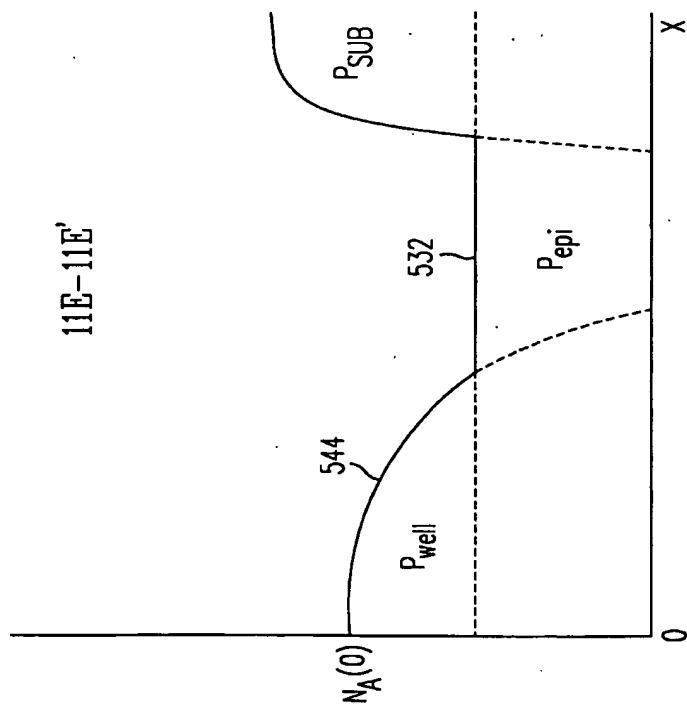
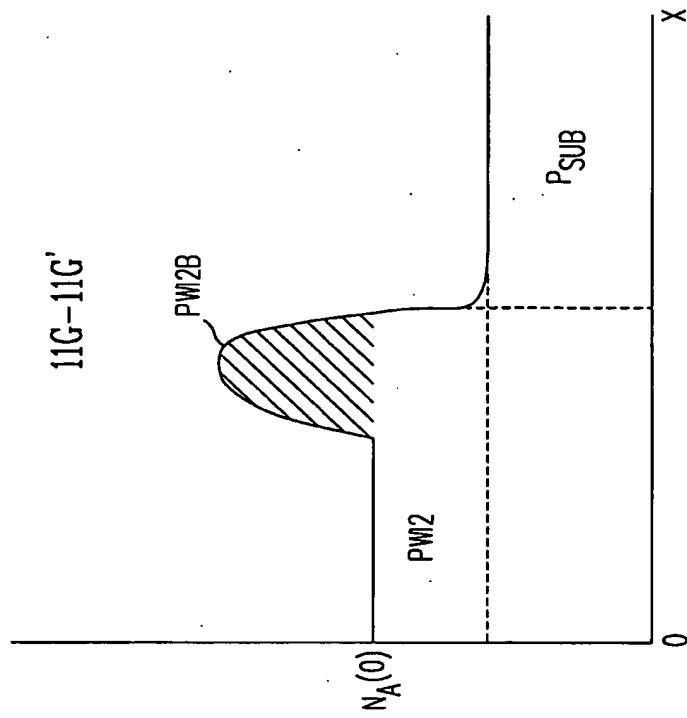


FIG. 11J

FIG. 11I

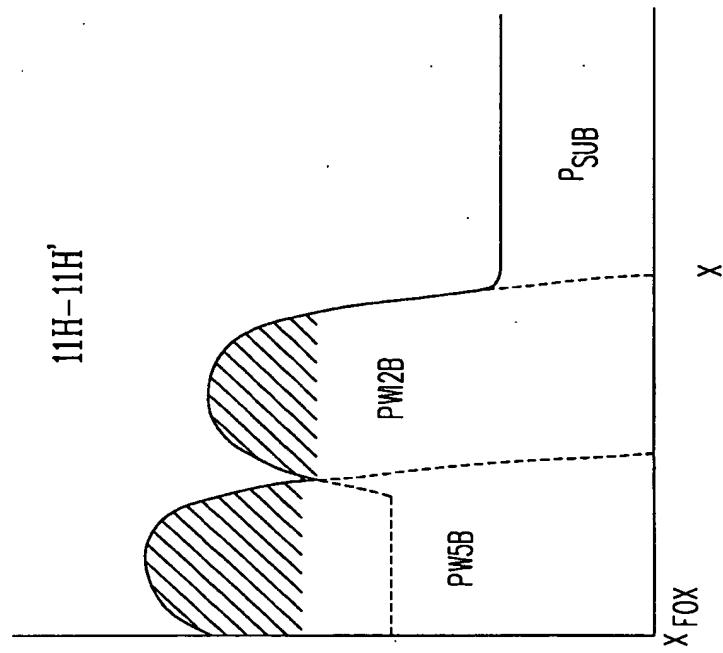


FIG. 11L

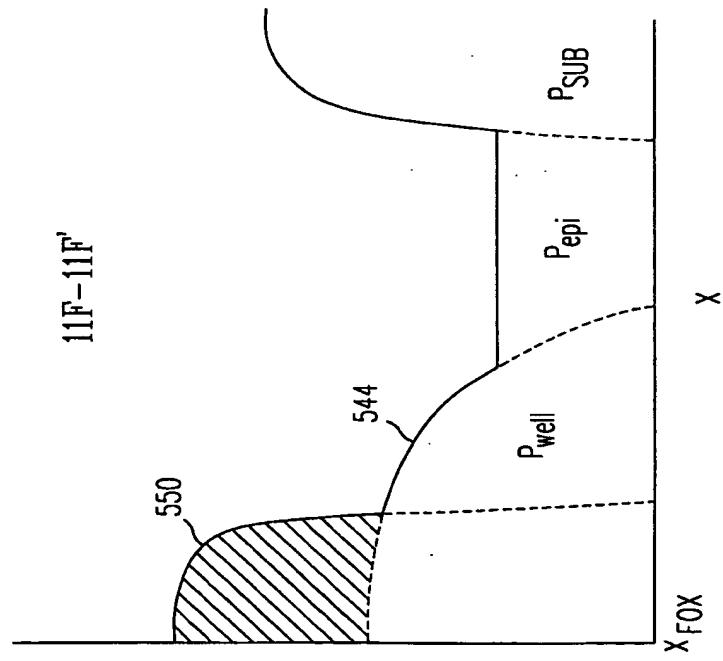


FIG. 11K

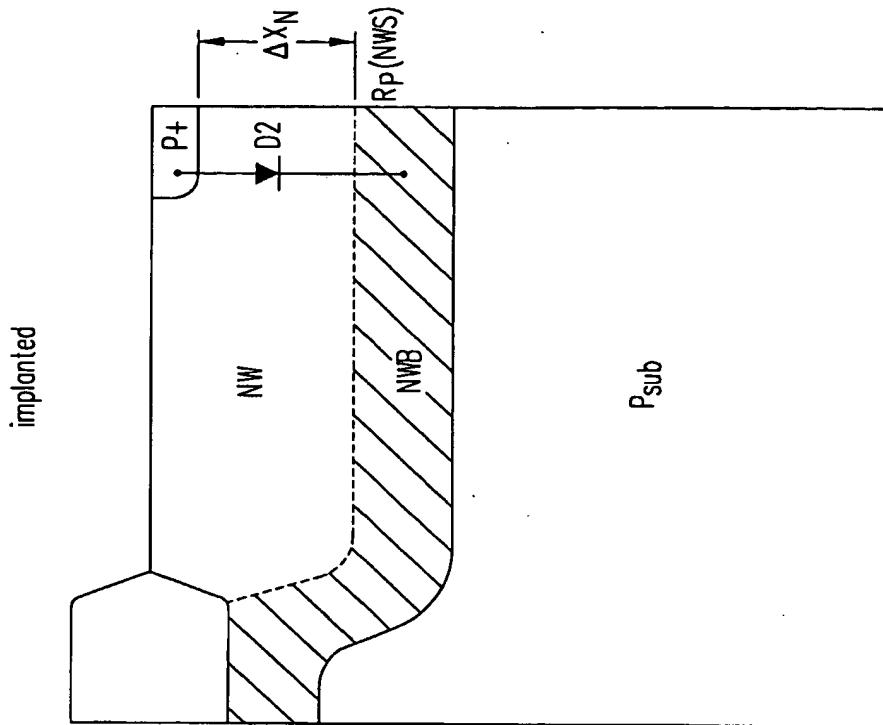


FIG. 12B

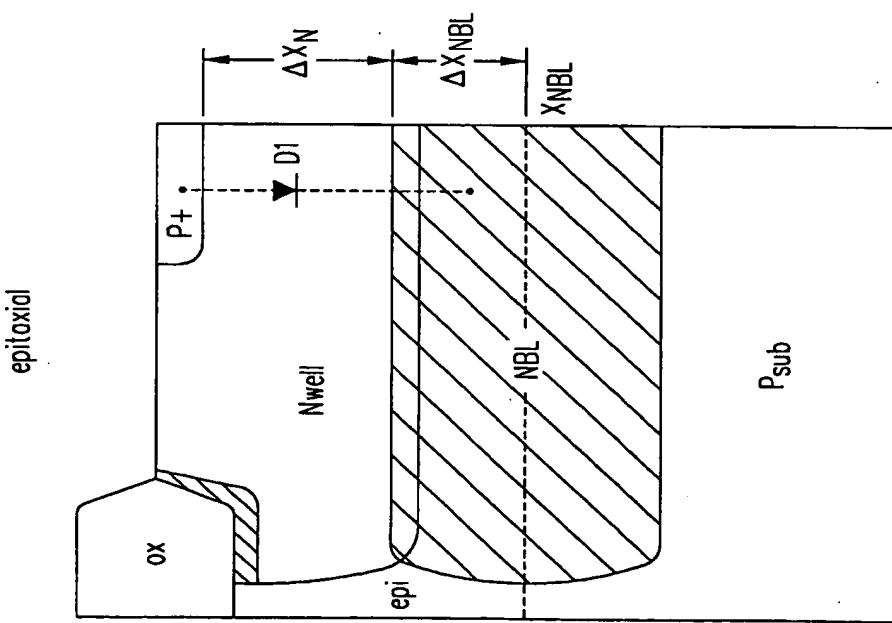


FIG. 12A

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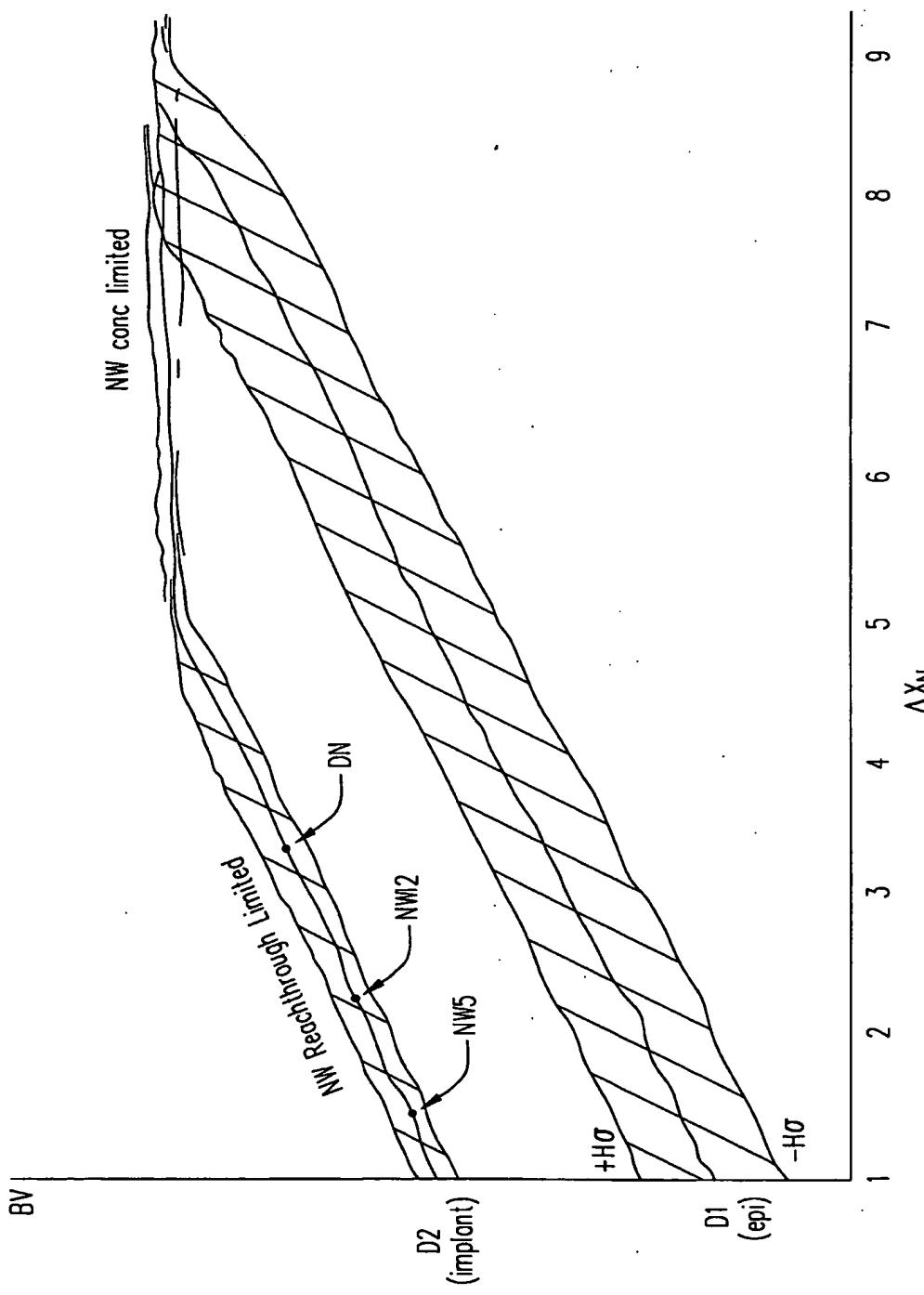


FIG. 12C

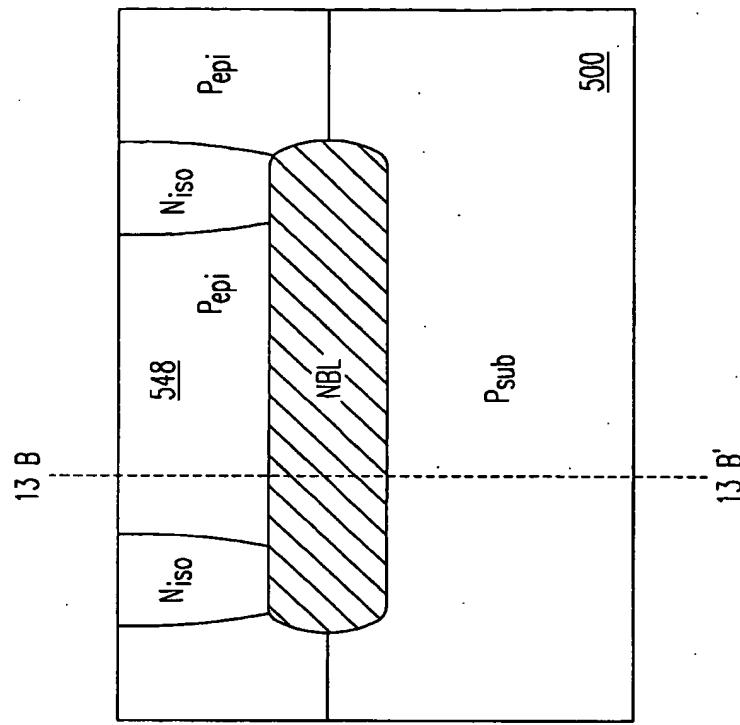


FIG. 13B
(Prior Art)

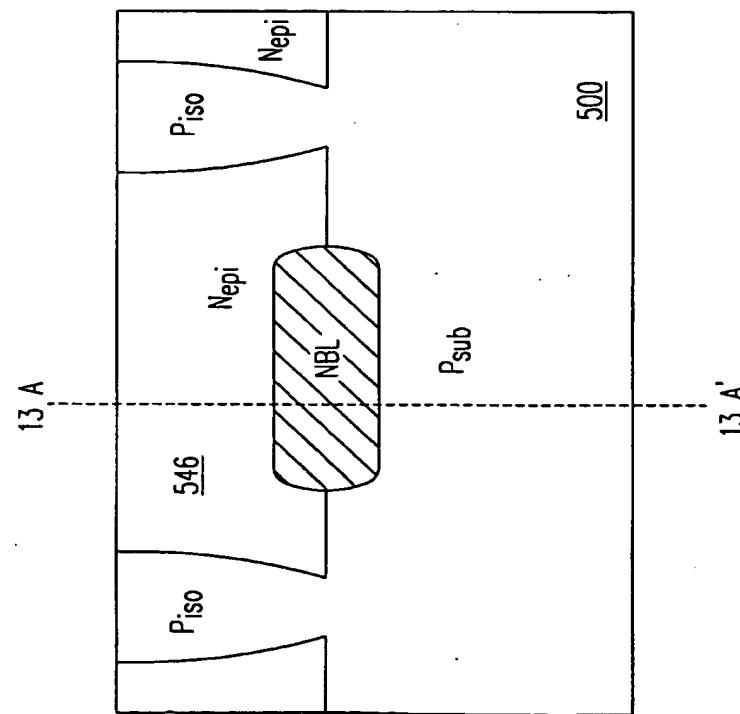
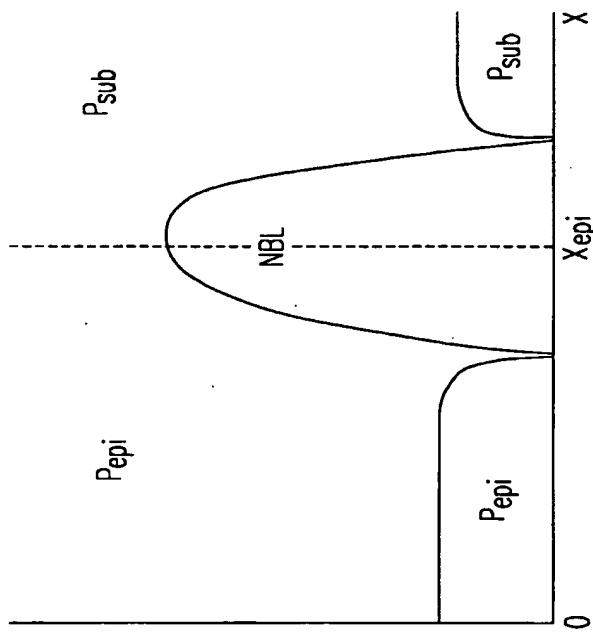


FIG. 13A
(Prior Art)

13B-13B'



13A-13A'

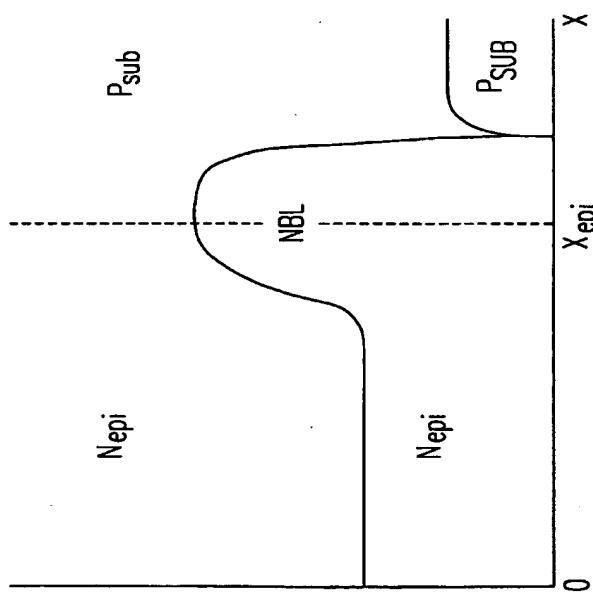


FIG. 13C

FIG. 13D

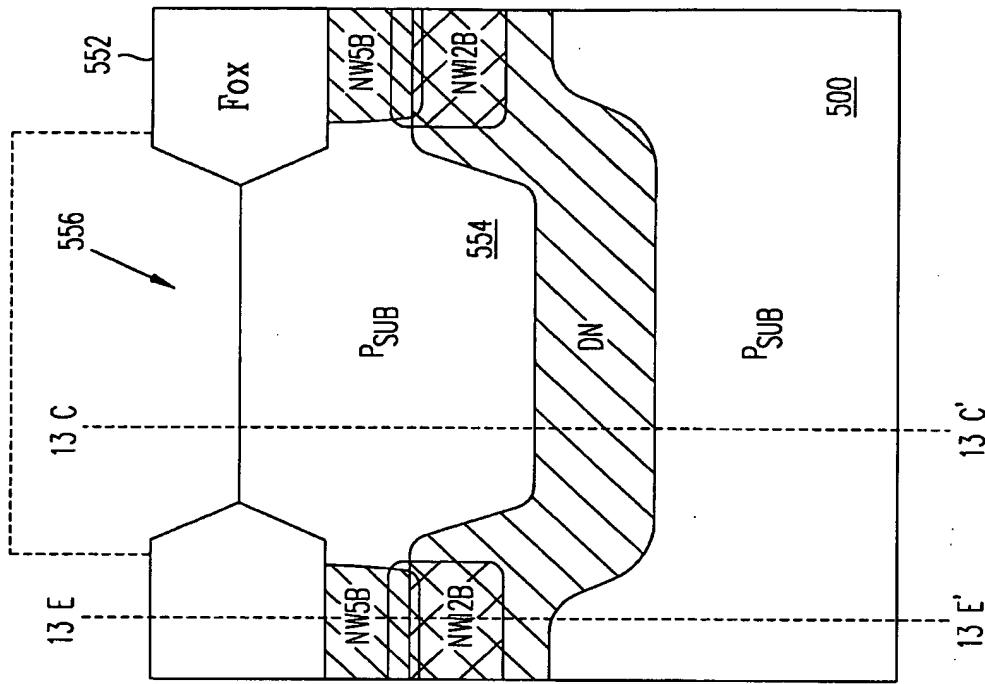


FIG. 13F

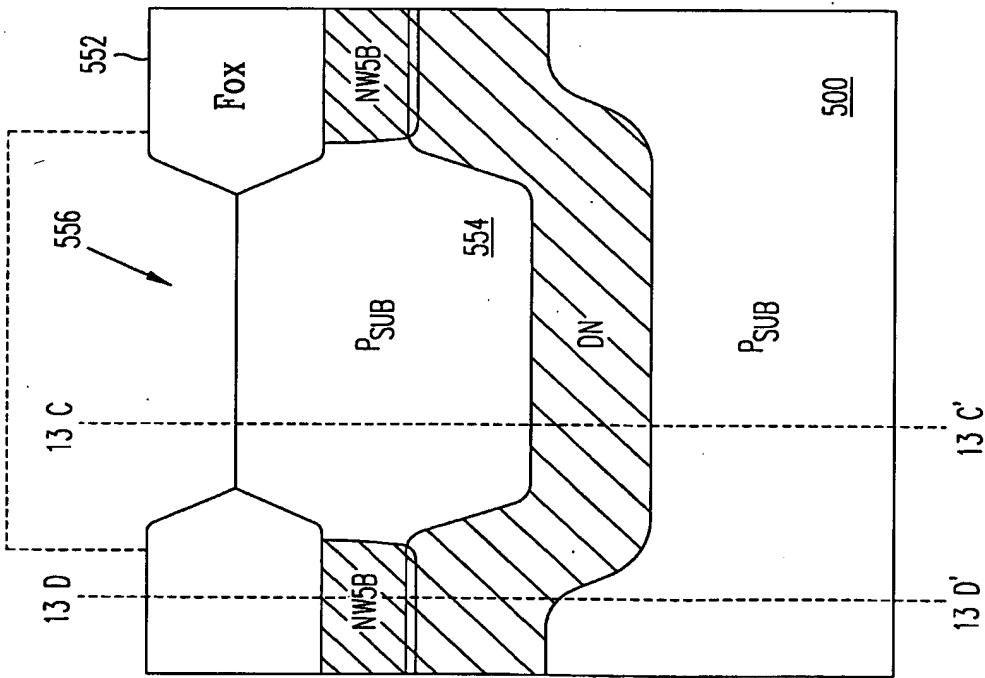
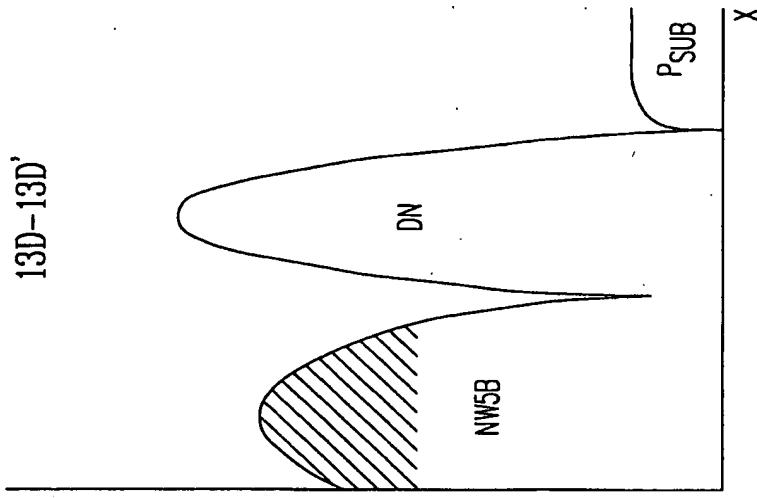


FIG. 13E

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13D-13D'



13C-13C'

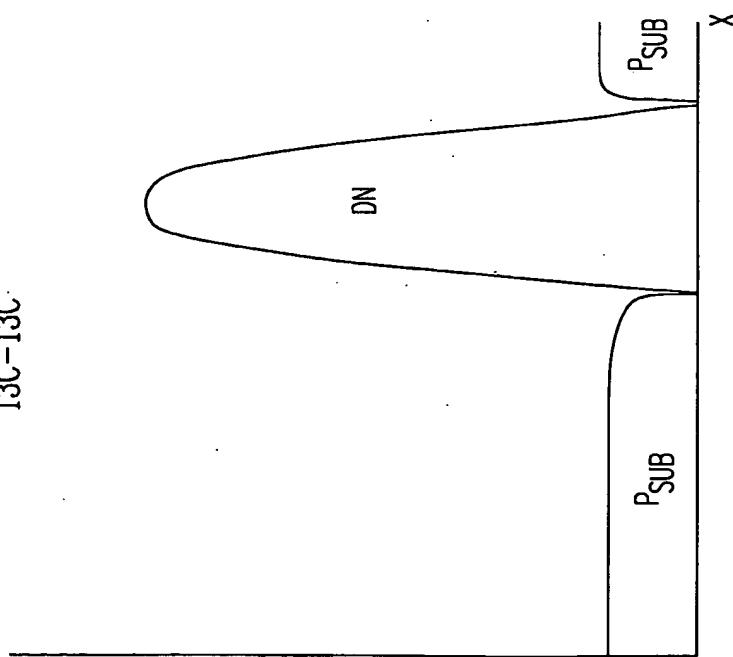


FIG. 13H

FIG. 13G

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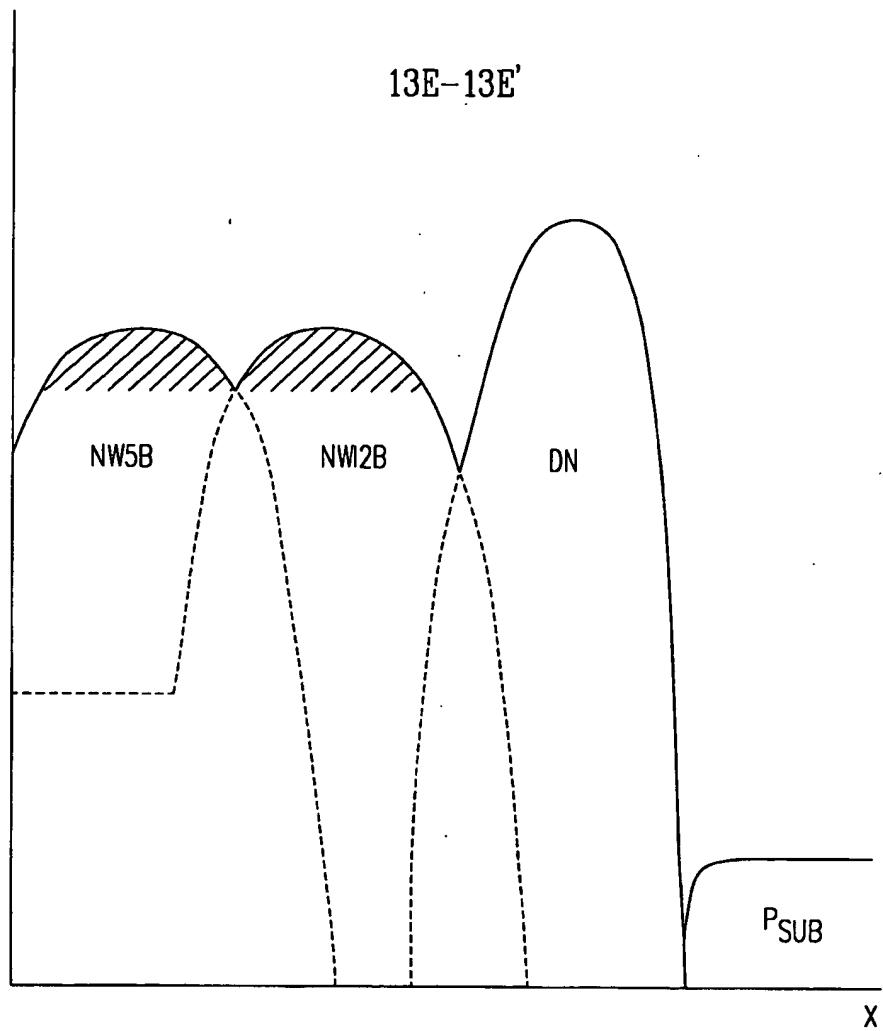


FIG. 13I

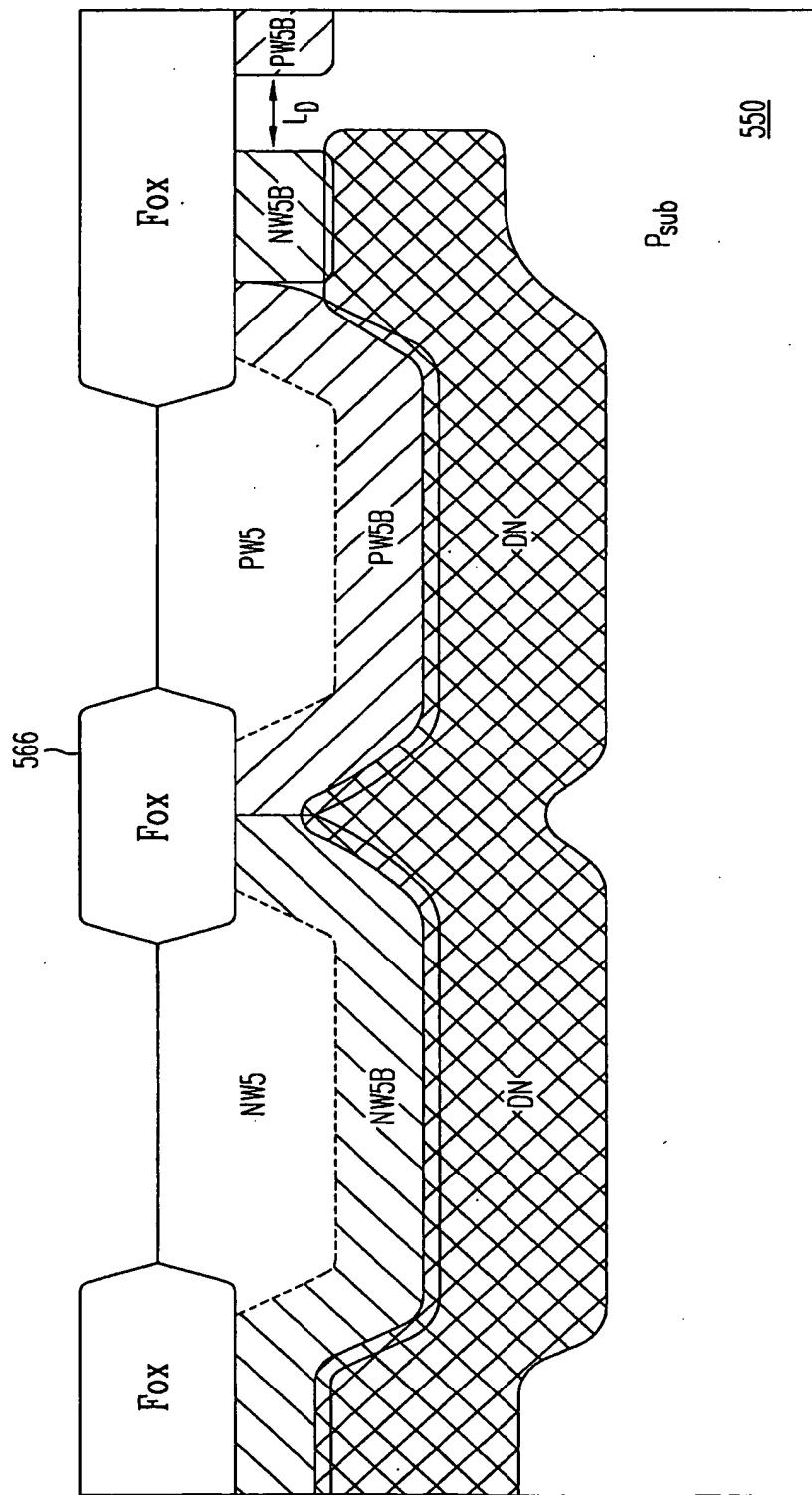


FIG. 14A

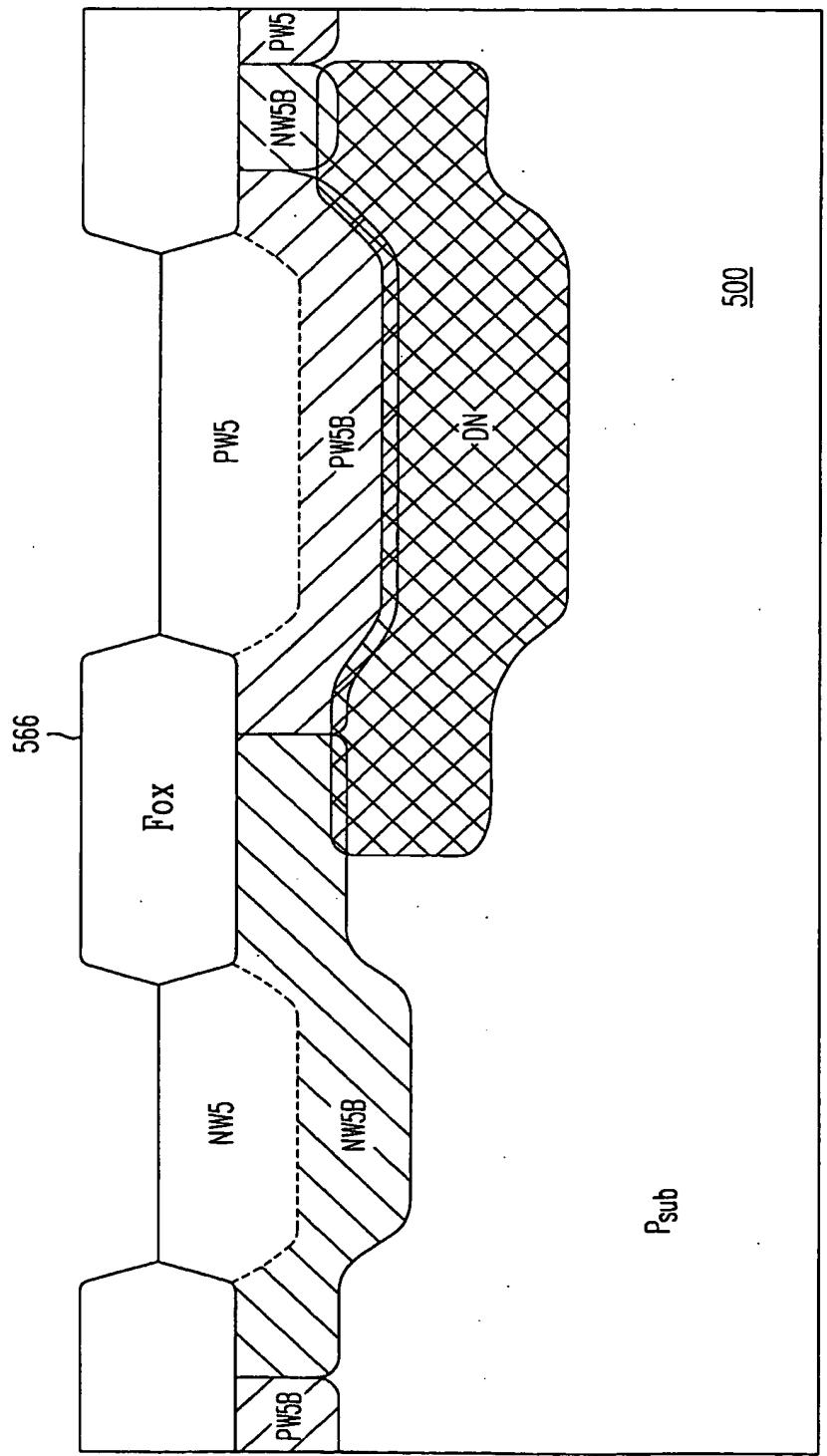


FIG. 14B

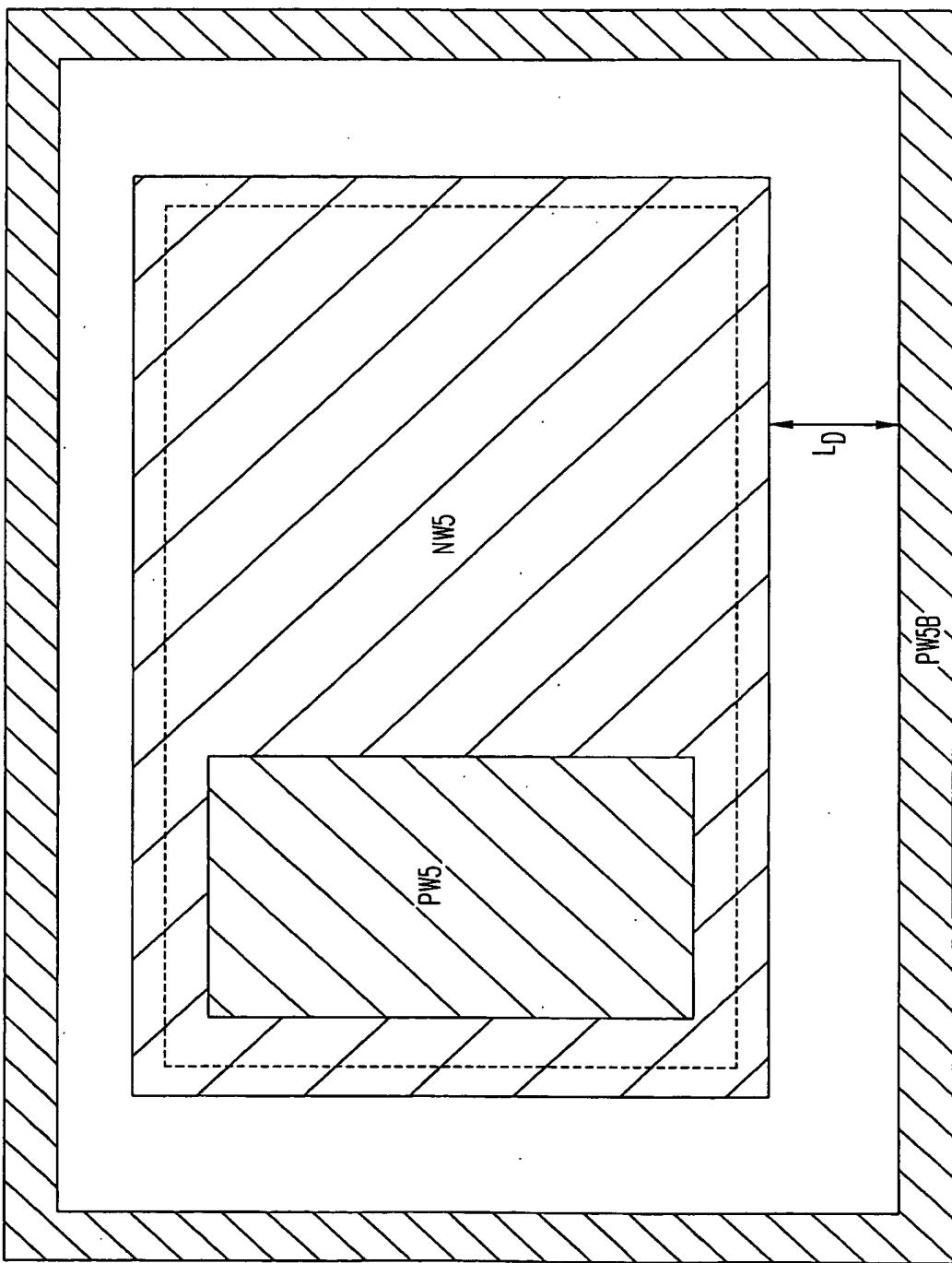


FIG. 14C

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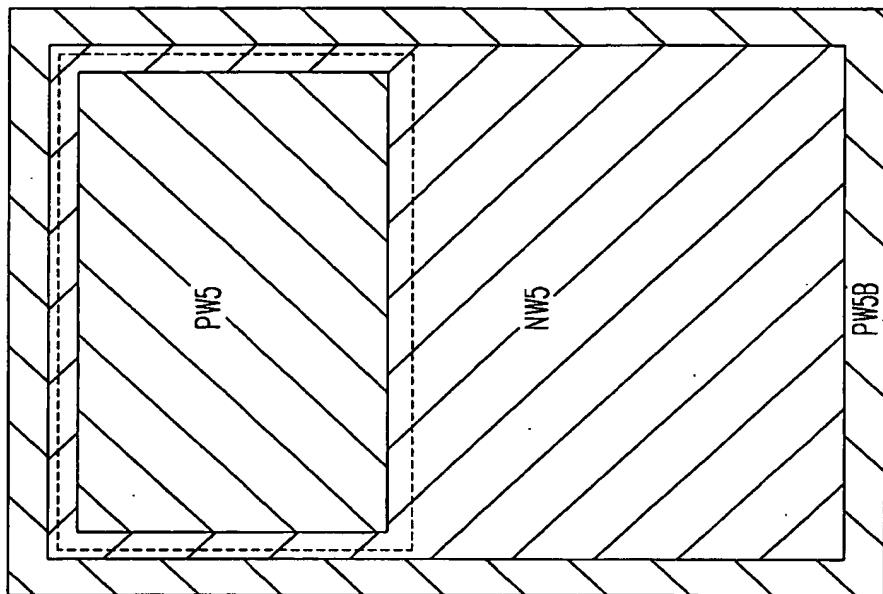


FIG. 14E

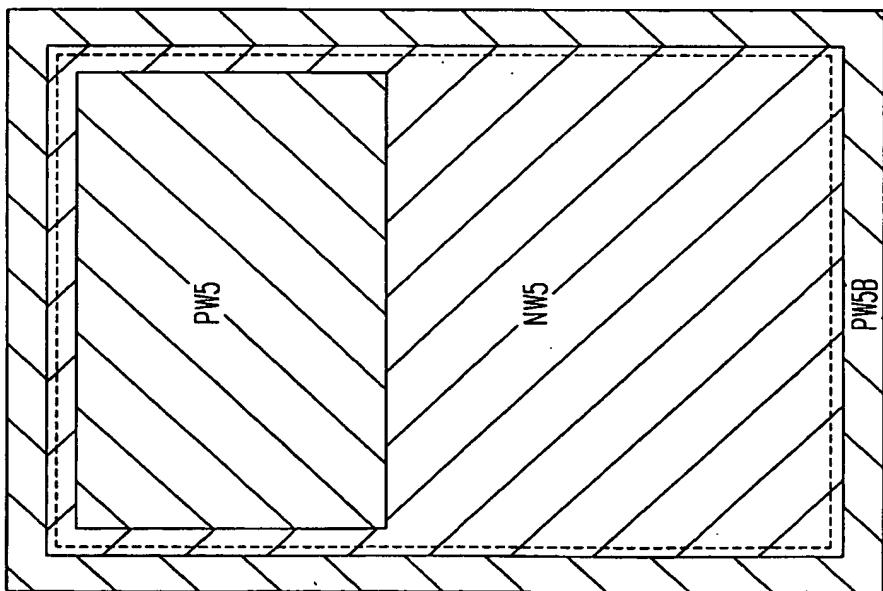


FIG. 14D

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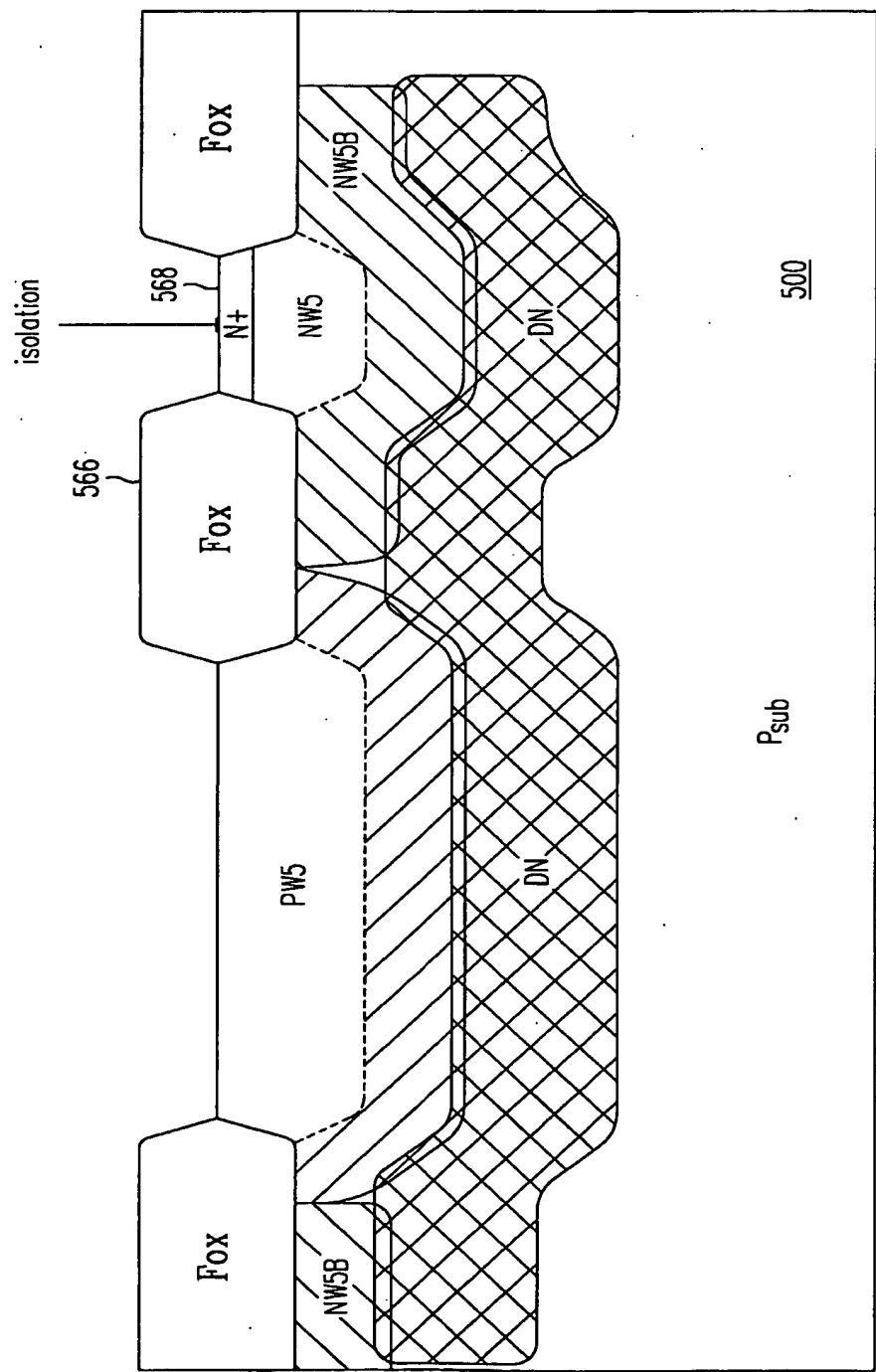


FIG. 14F

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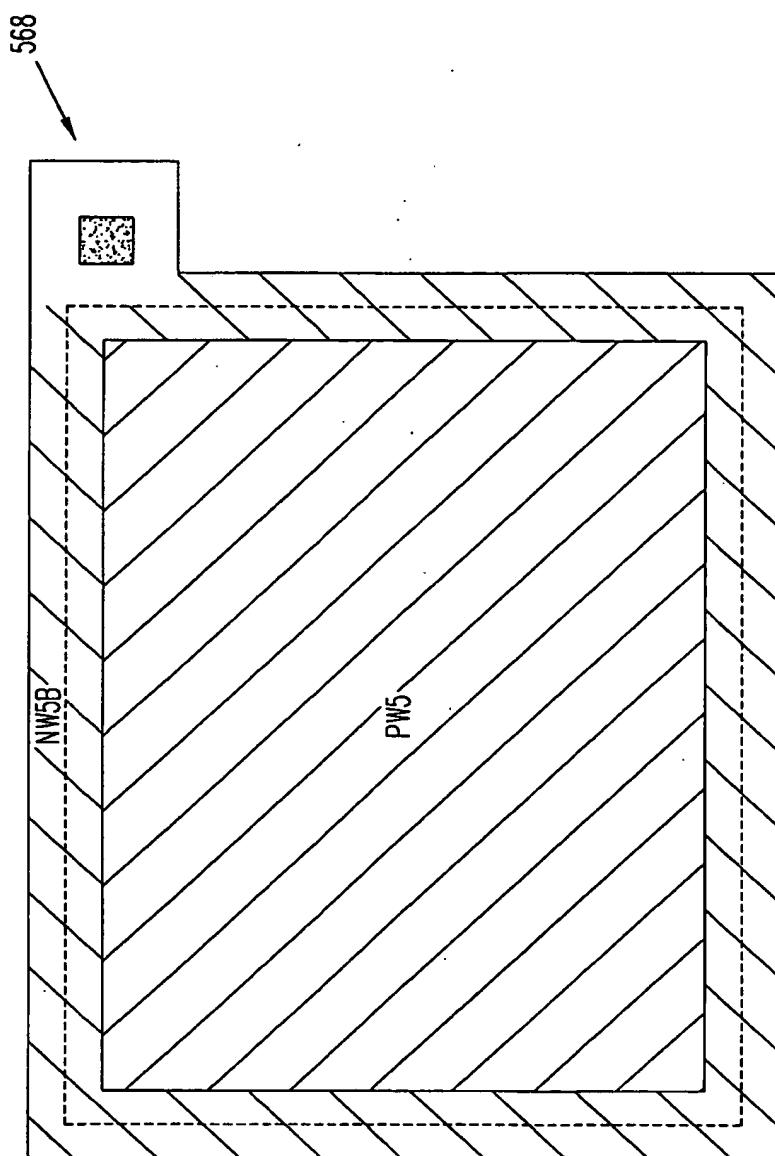


FIG. 14C

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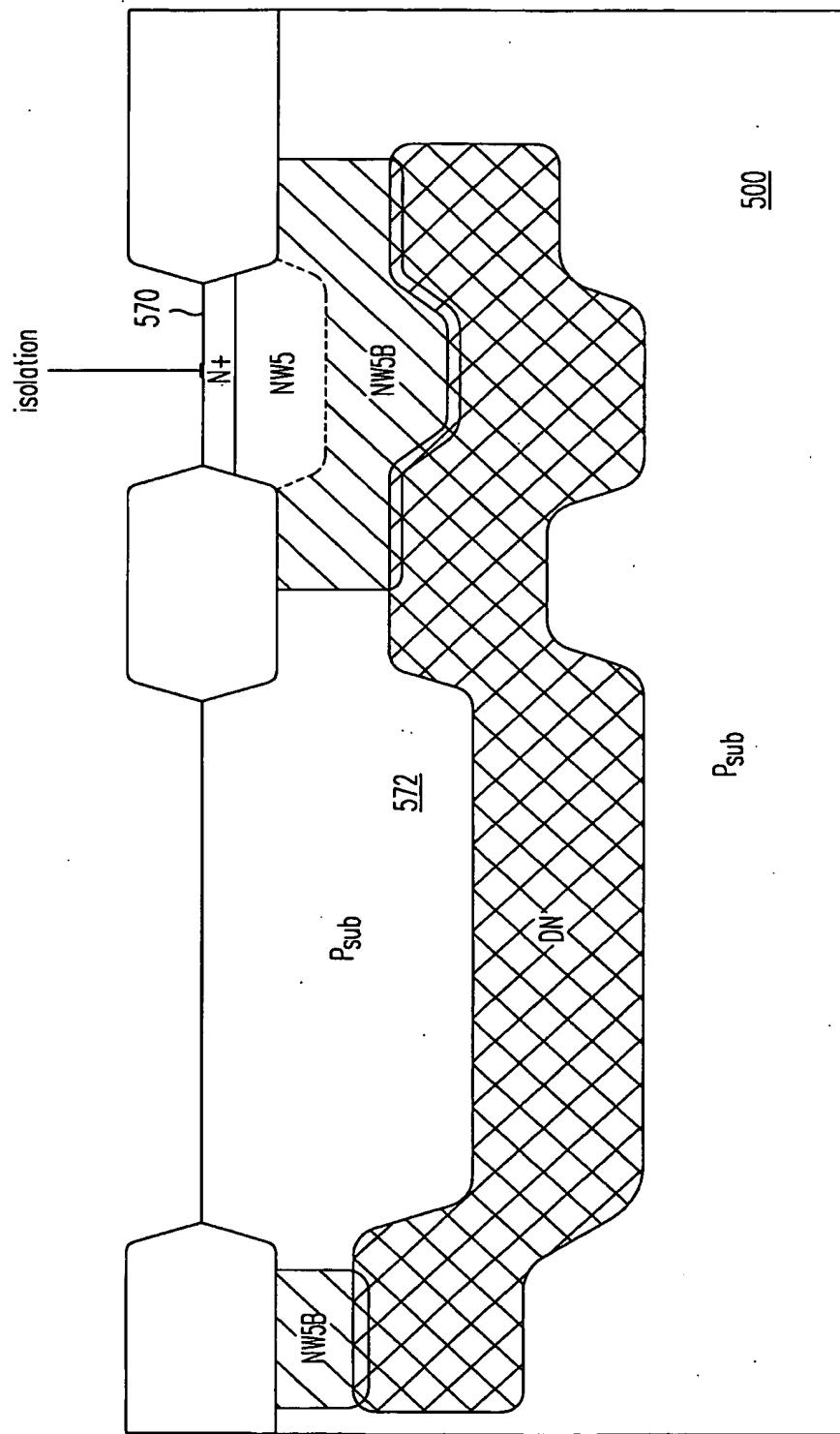


FIG. 14H

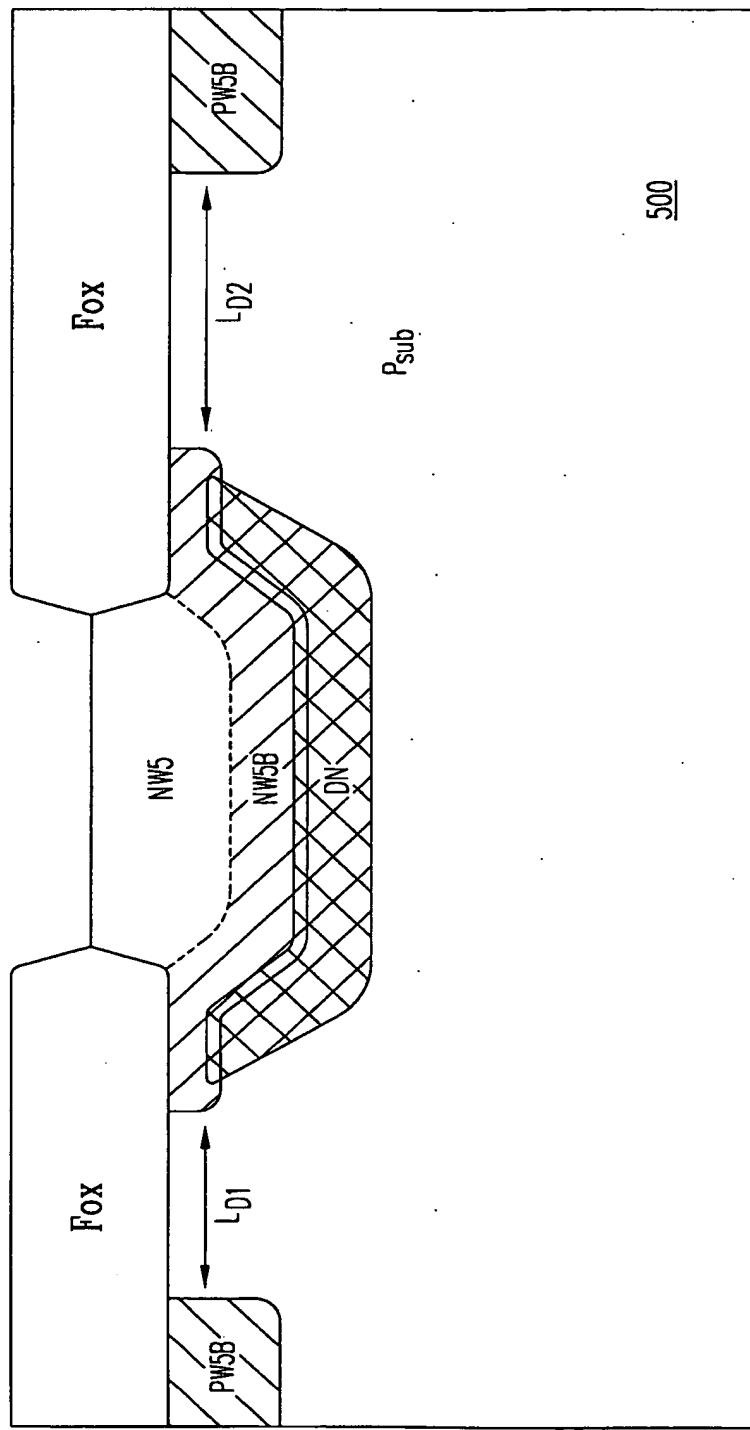


FIG. 14I

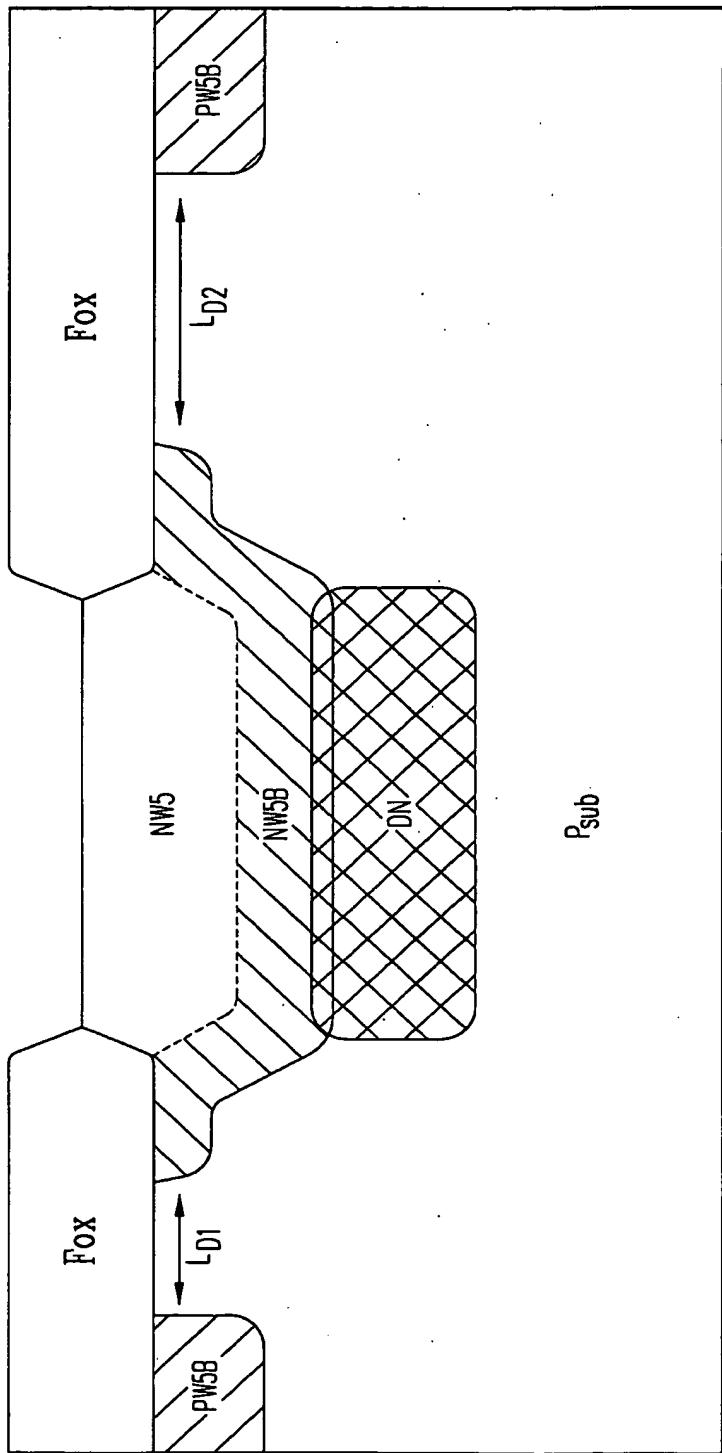


FIG. 14J

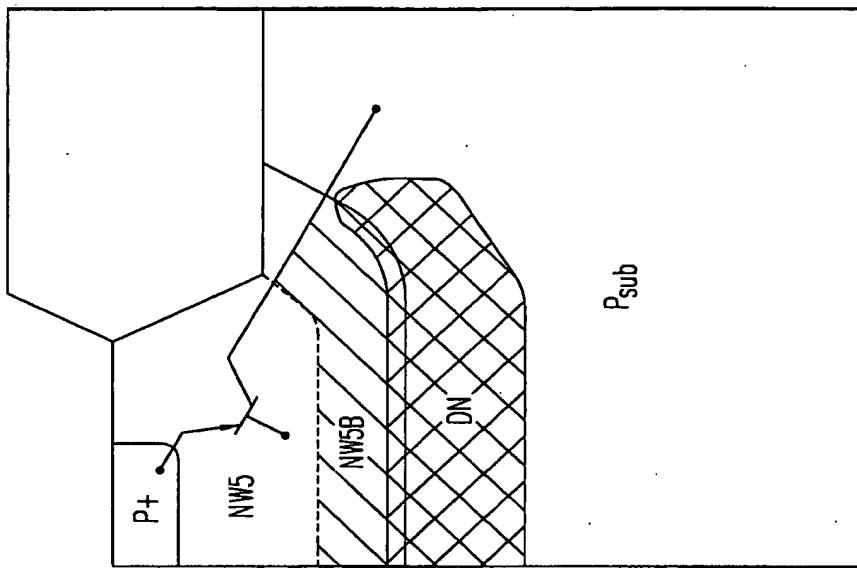


FIG. 14L

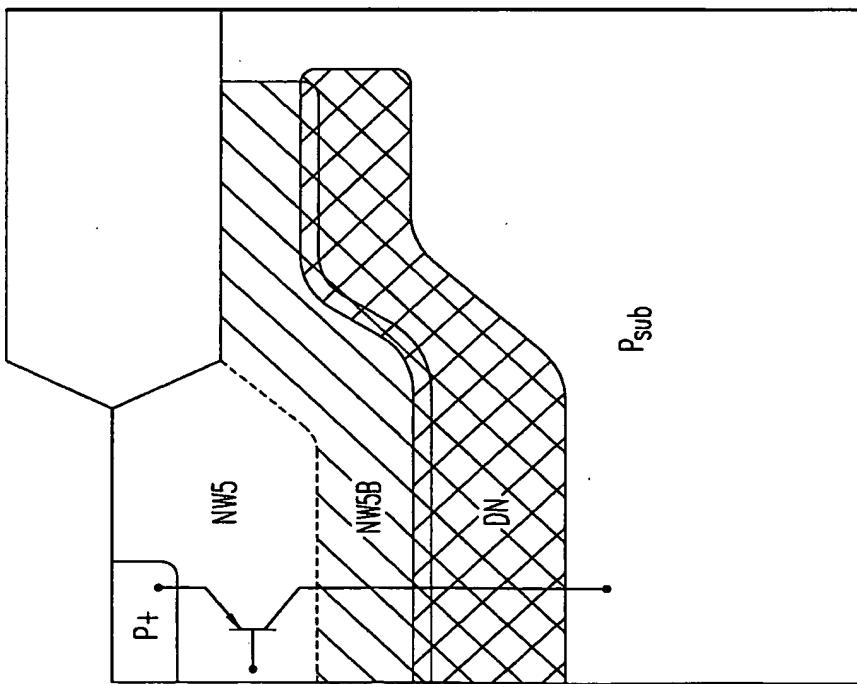


FIG. 14K

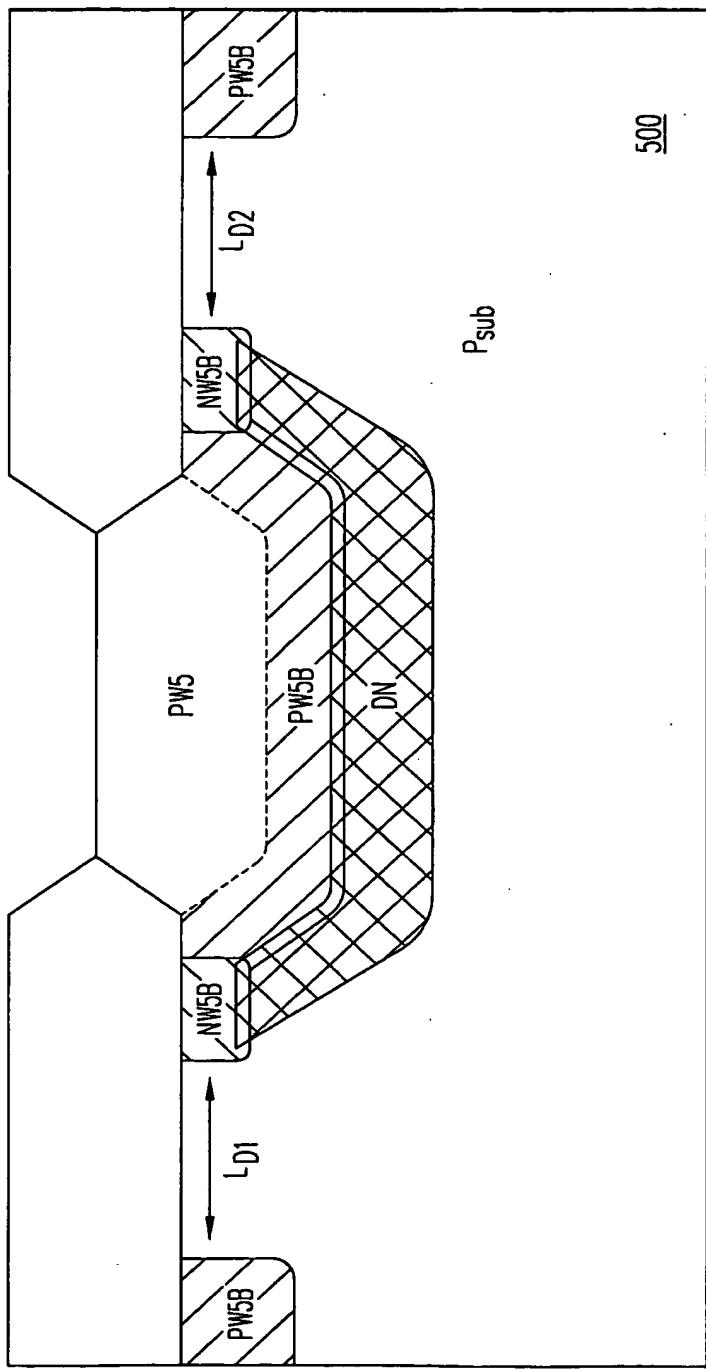


FIG. 14M

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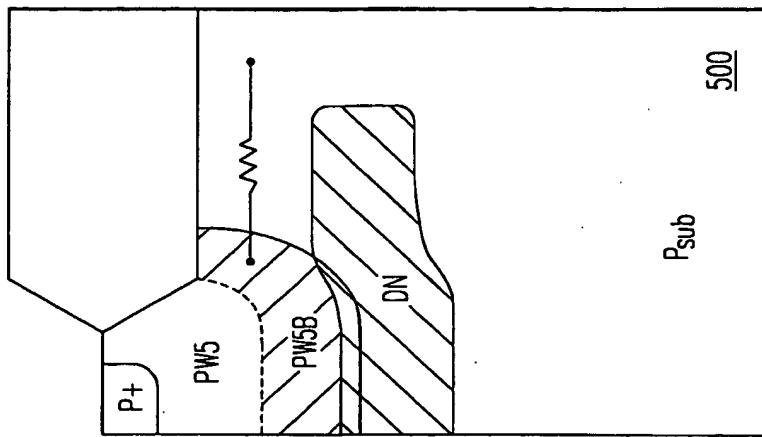


FIG. 14P

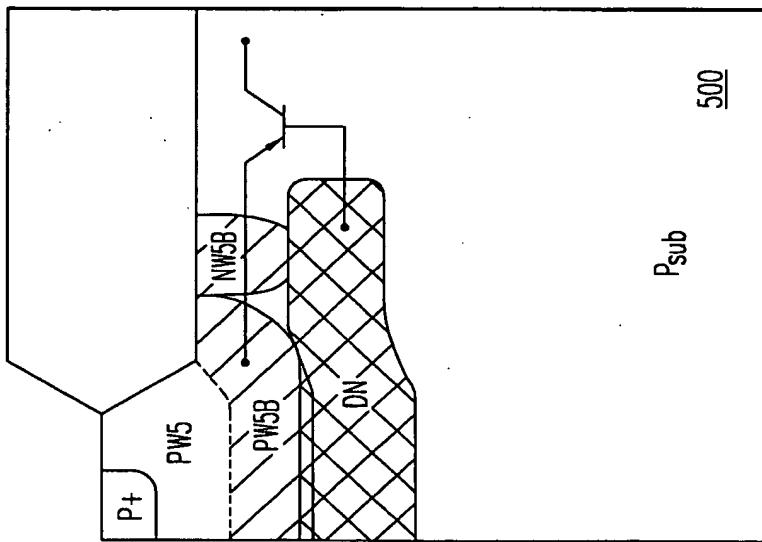


FIG. 14O

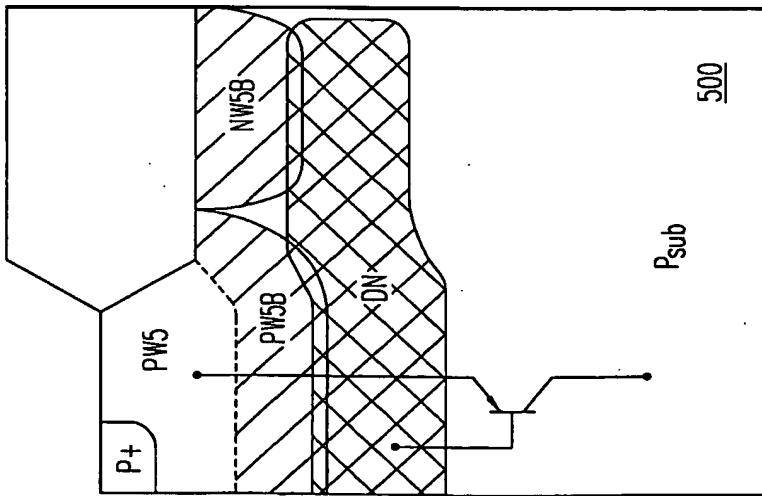


FIG. 14N

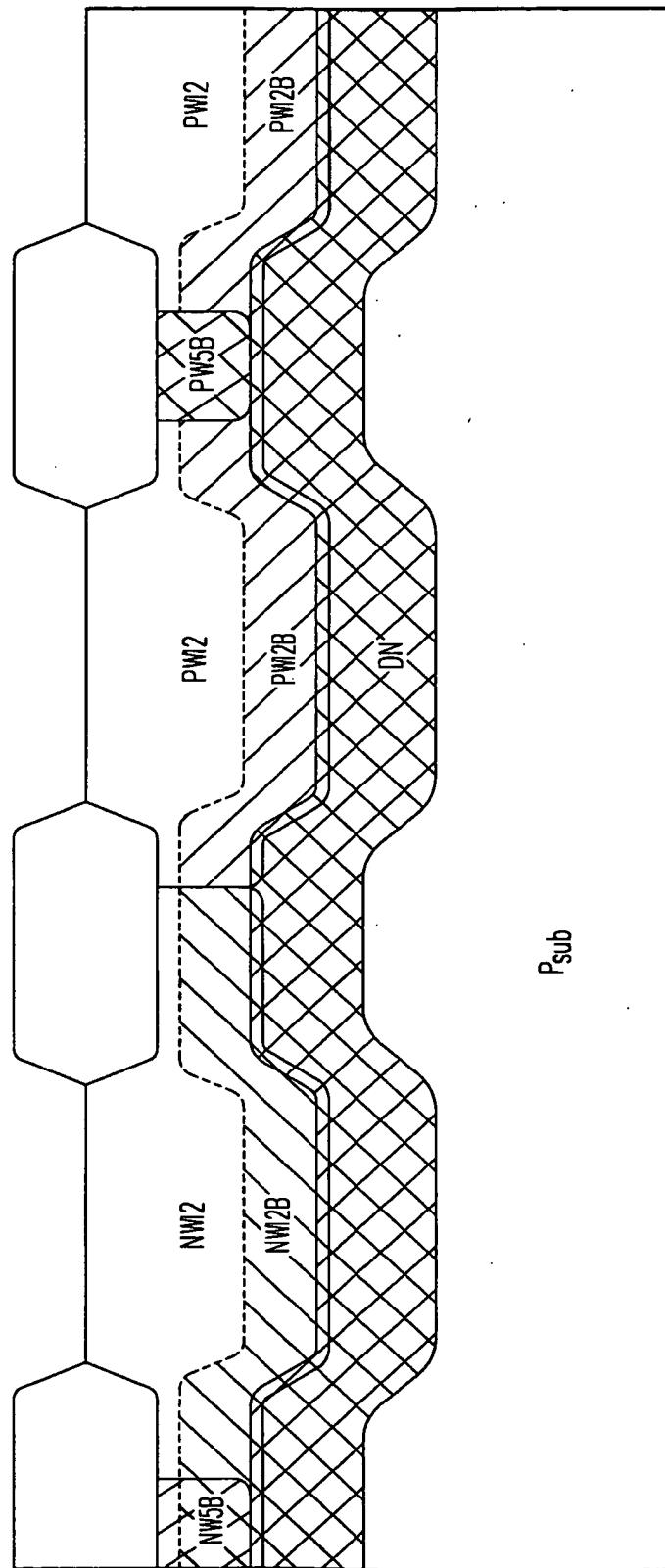


FIG. 15A

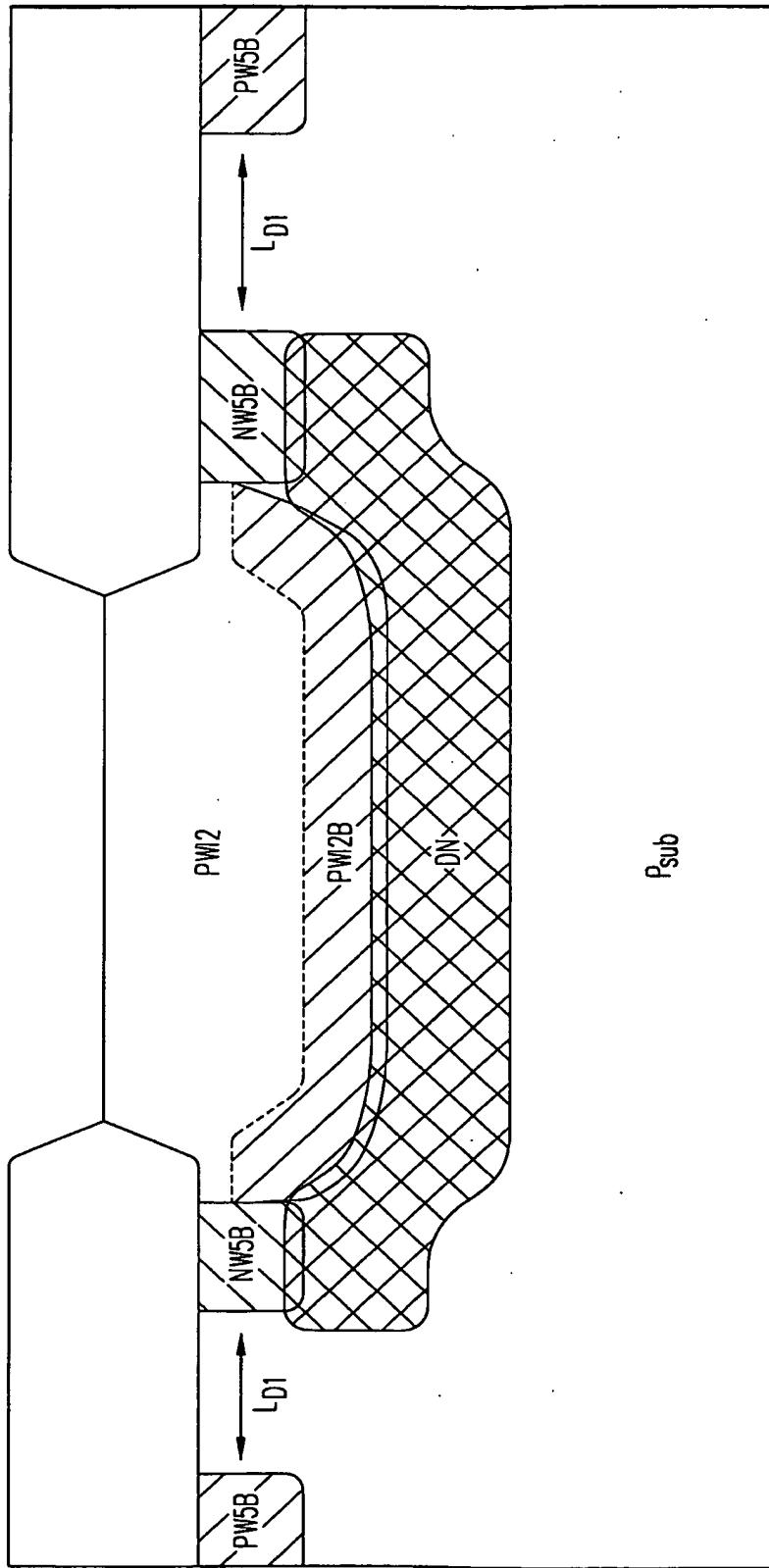


FIG. 15B

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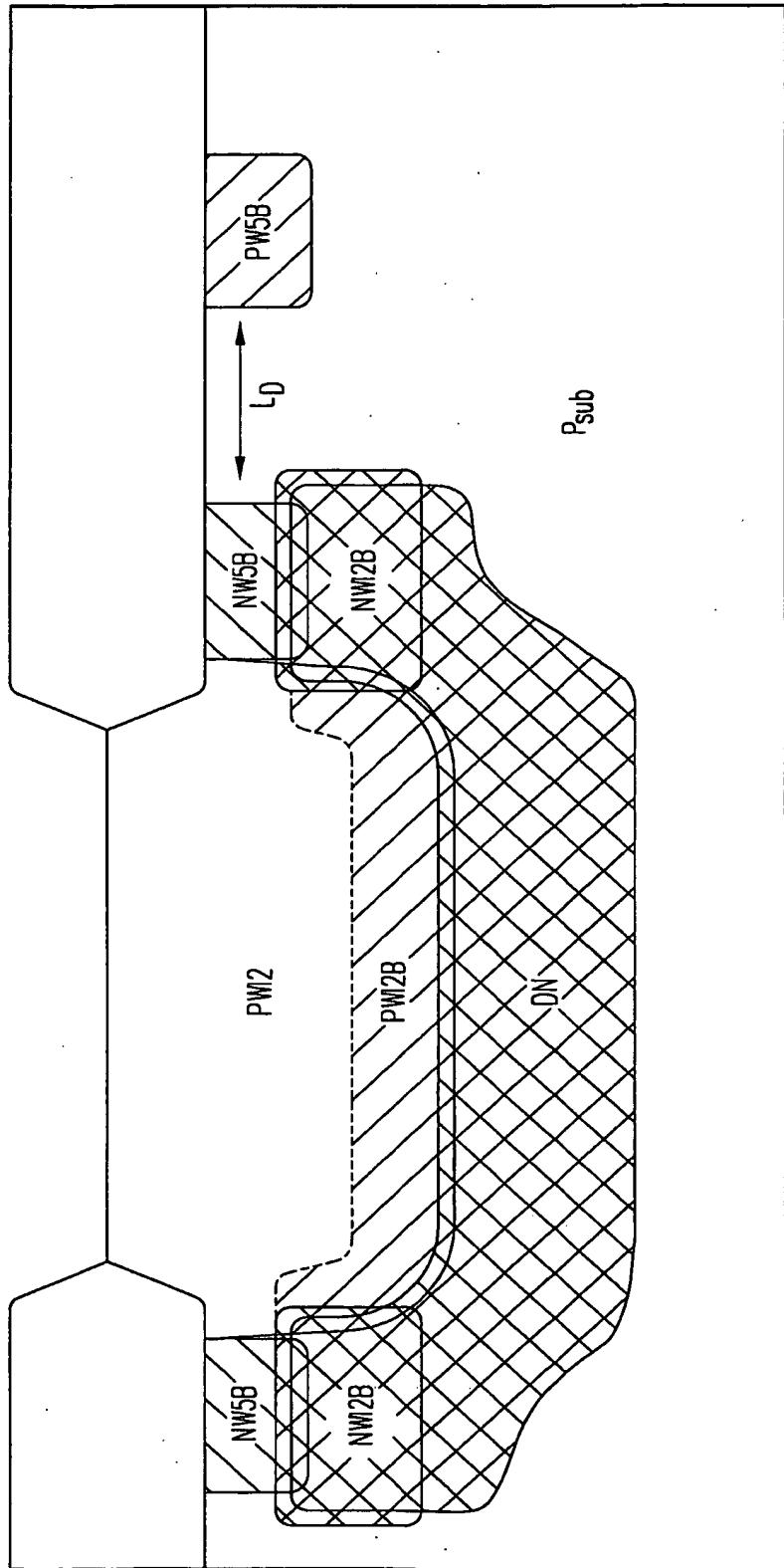


FIG. 15C

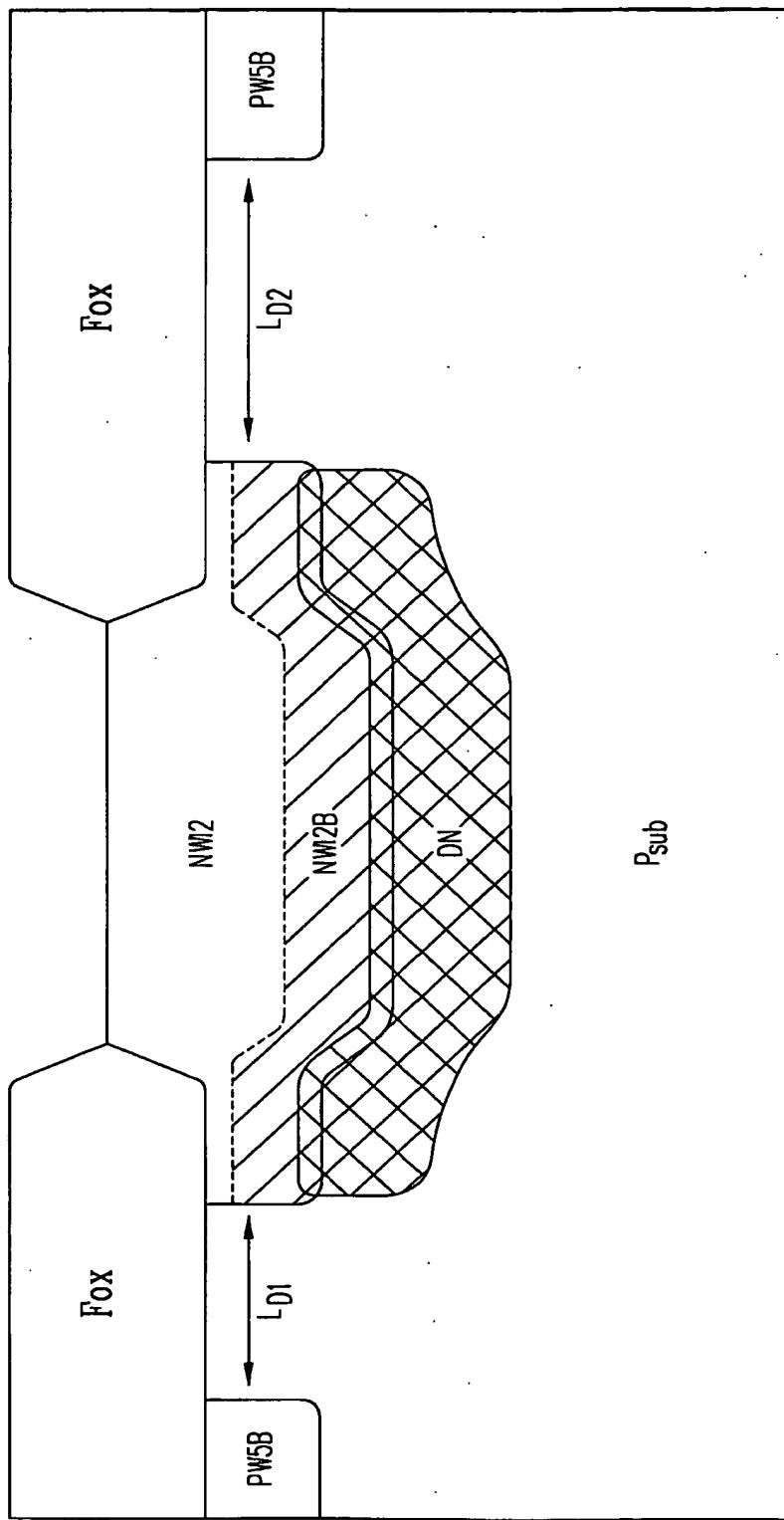


FIG. 15D

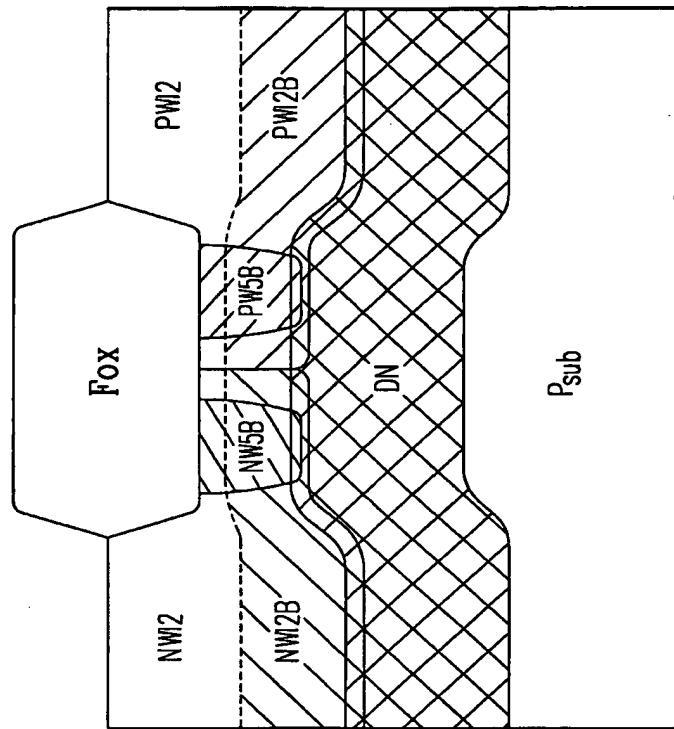


FIG. 15F

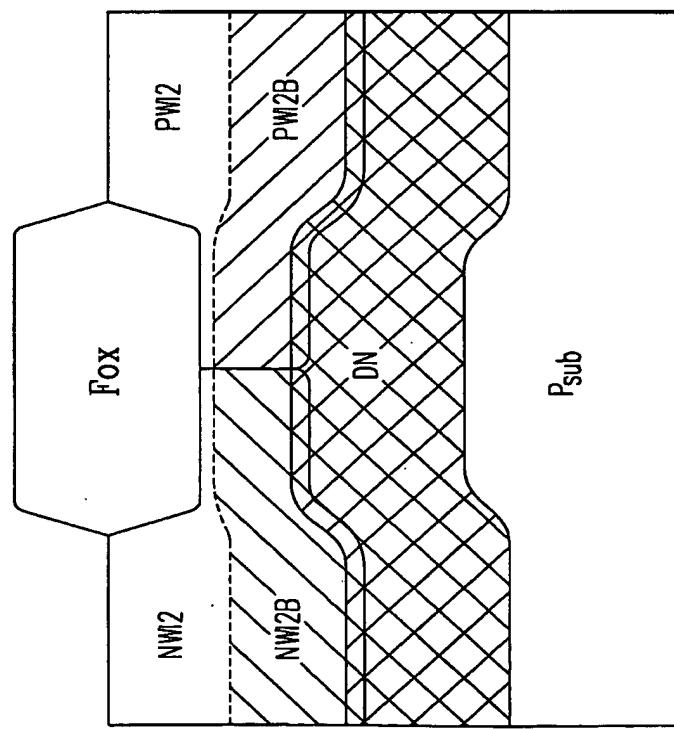


FIG. 15E

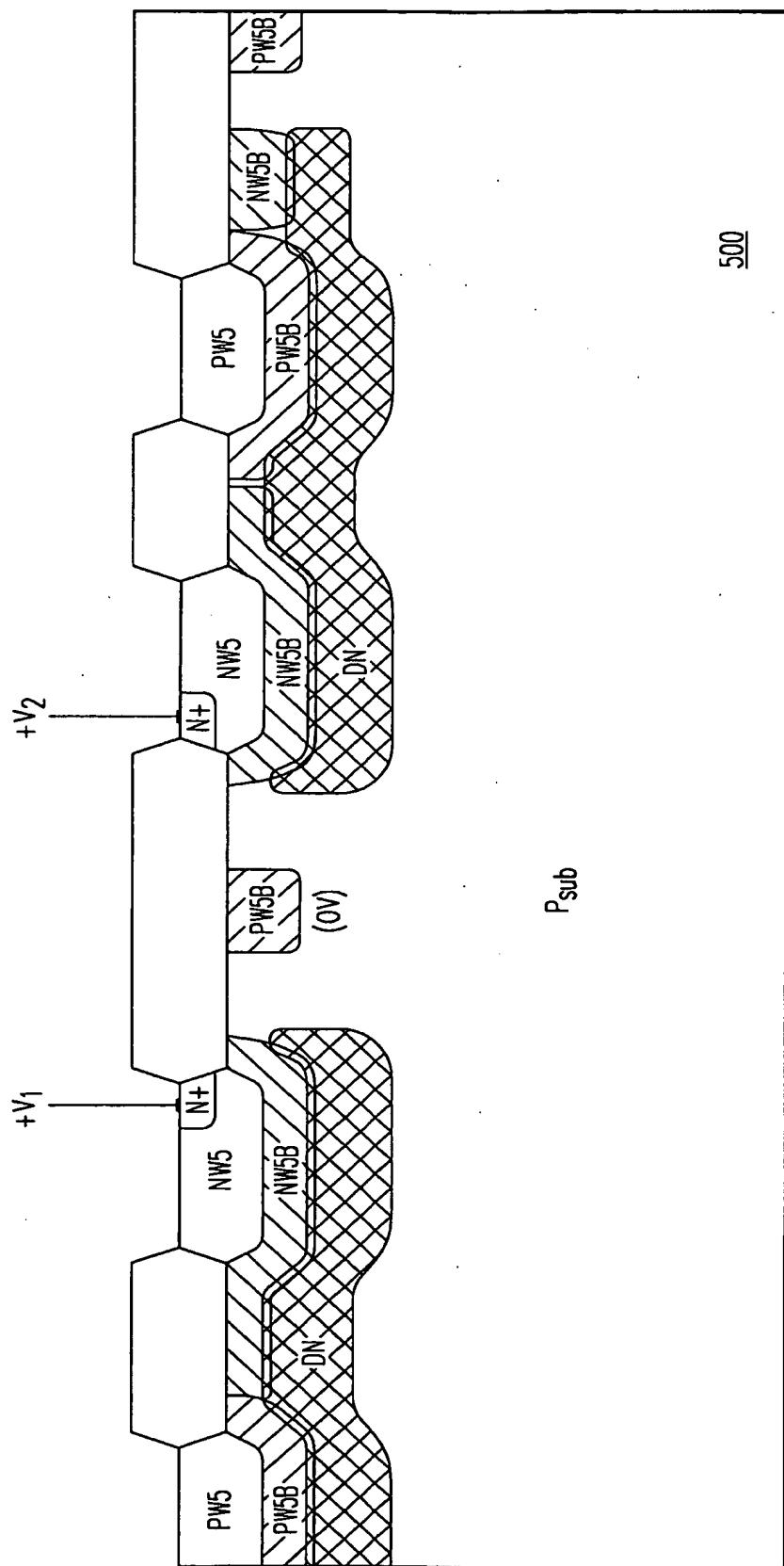


FIG. 16A

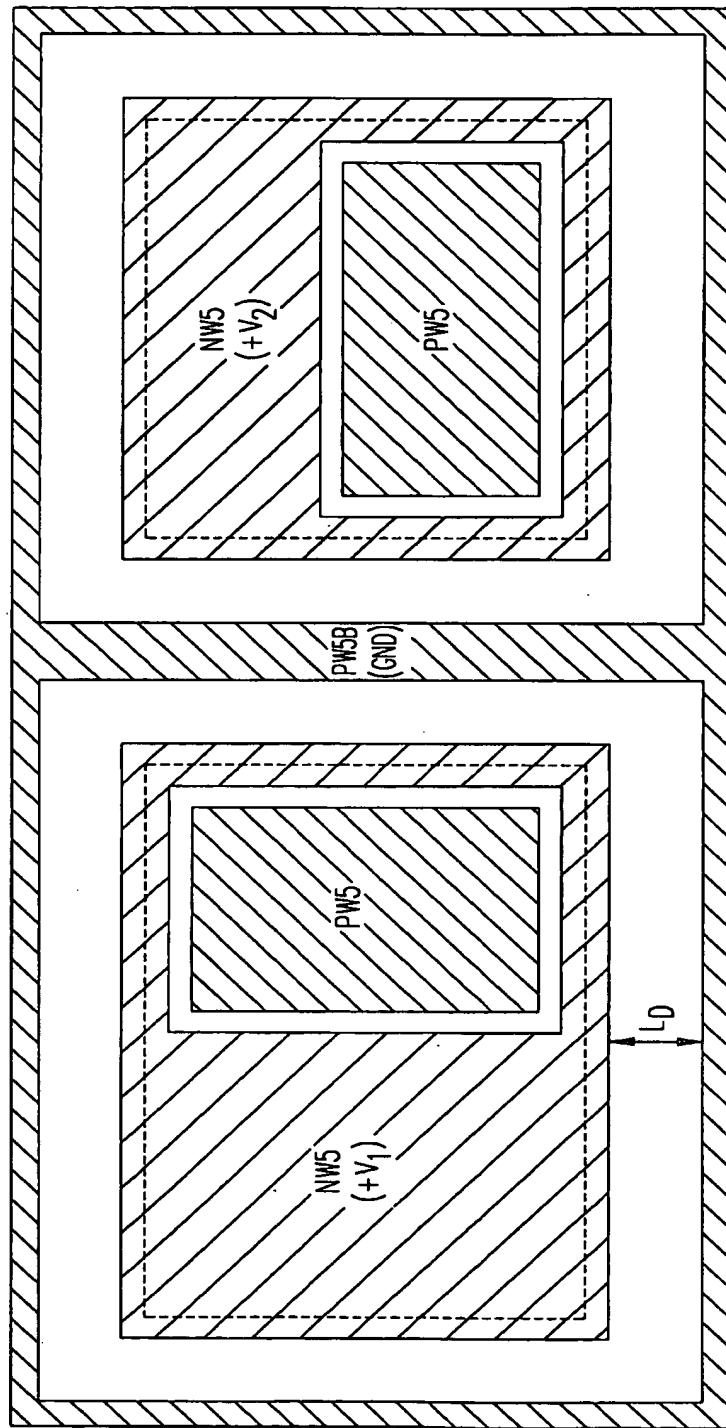


FIG. 16B

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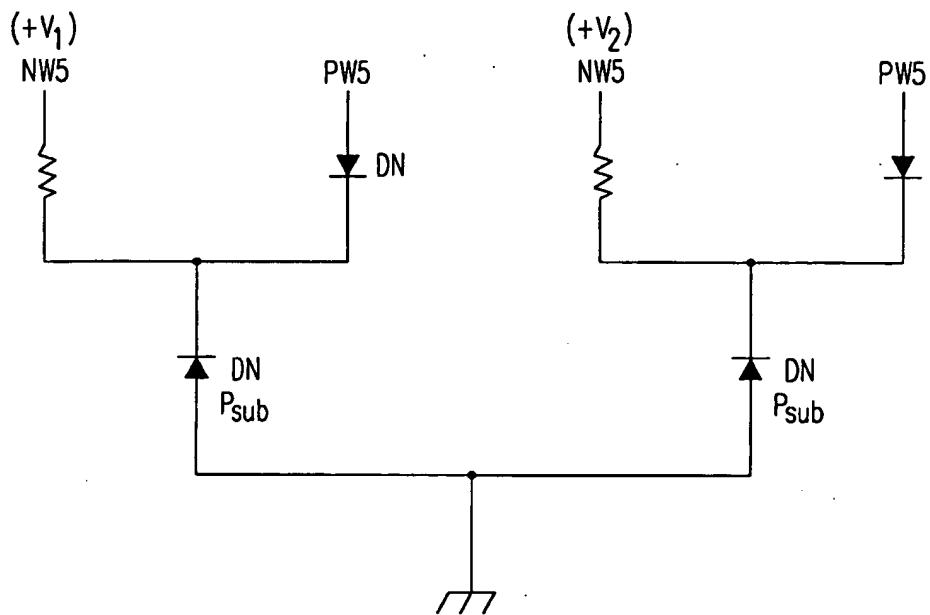


FIG. 16C

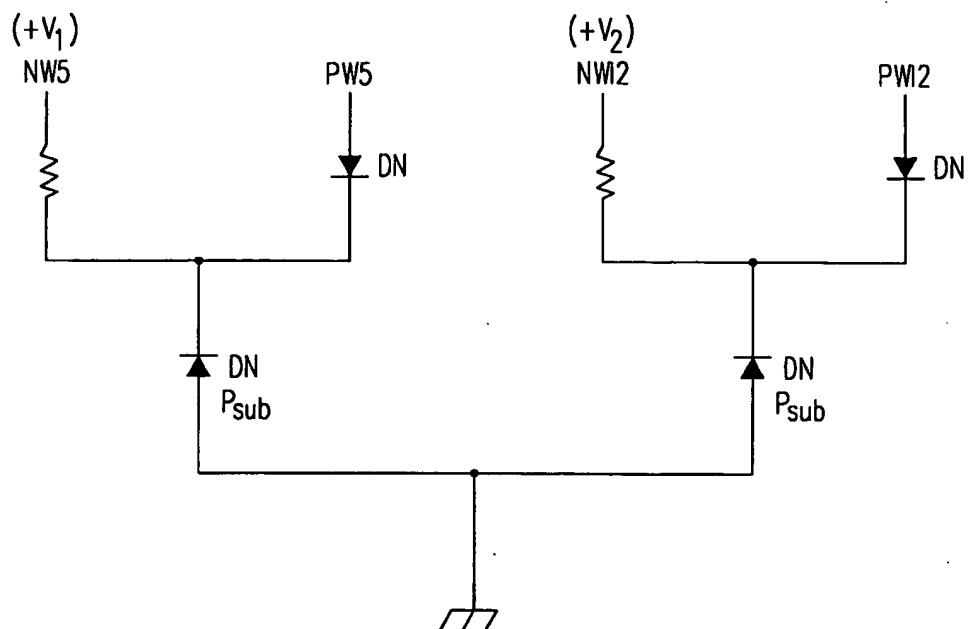


FIG. 16E

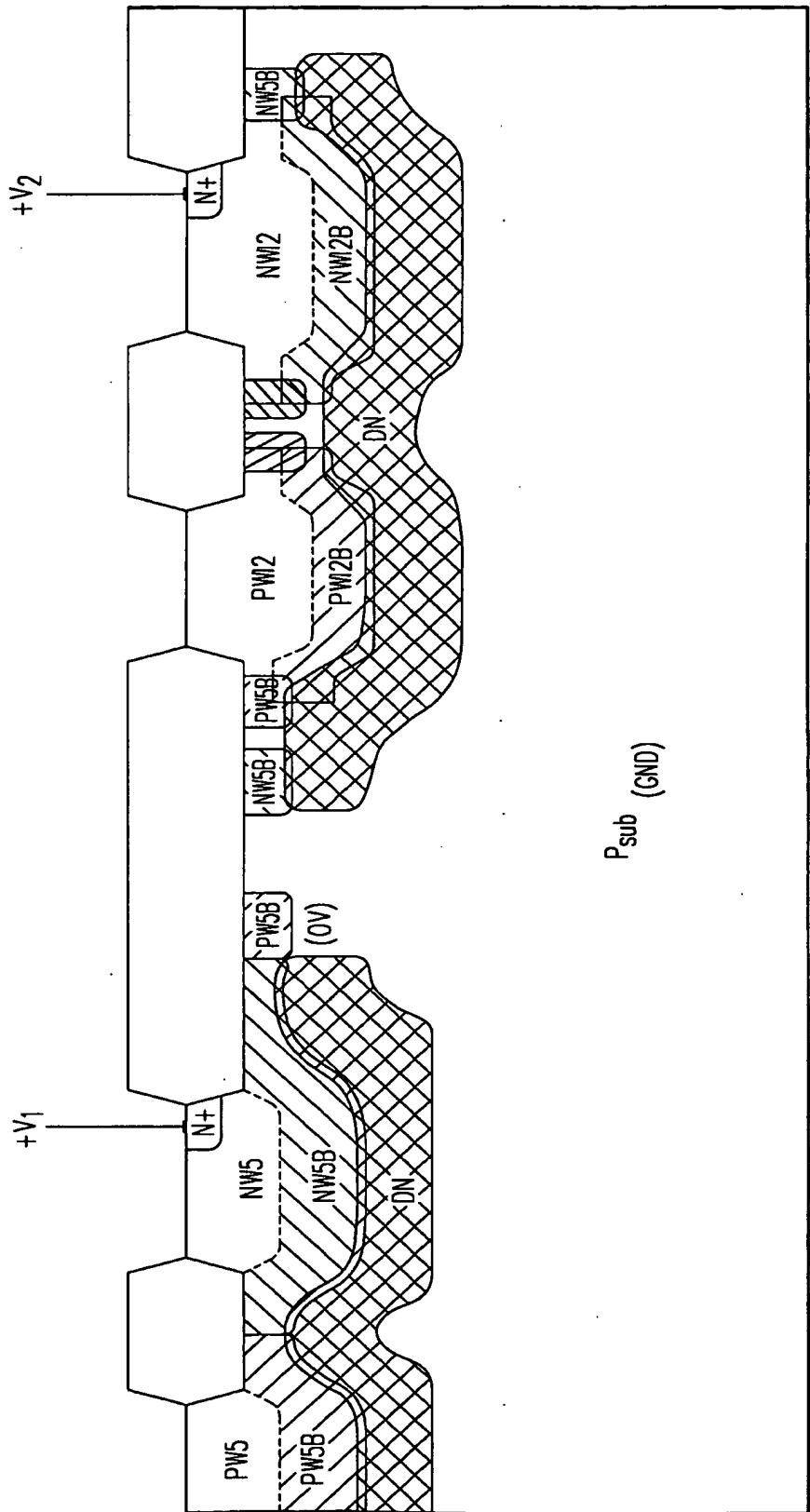


FIG. 16D

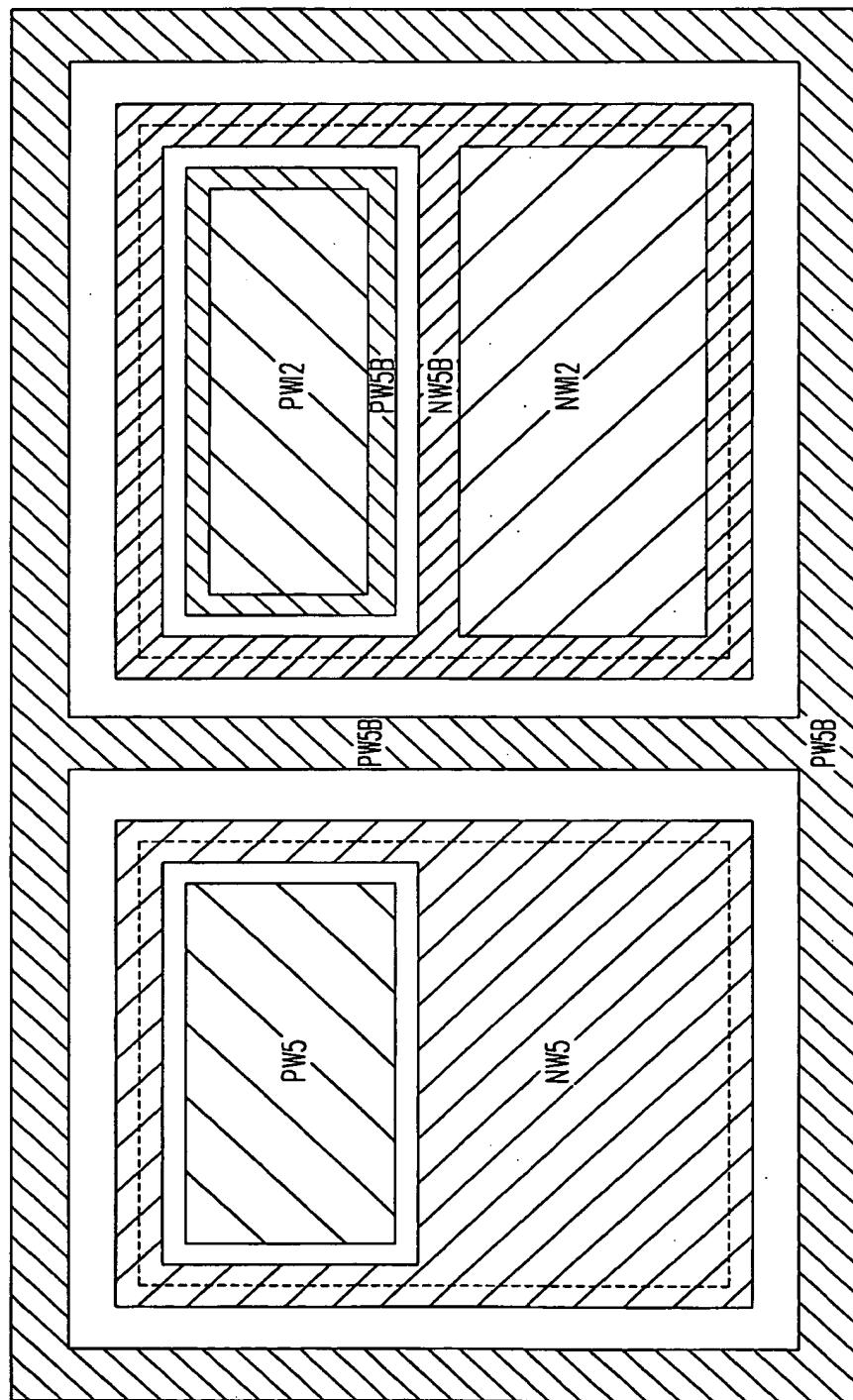


FIG. 16F

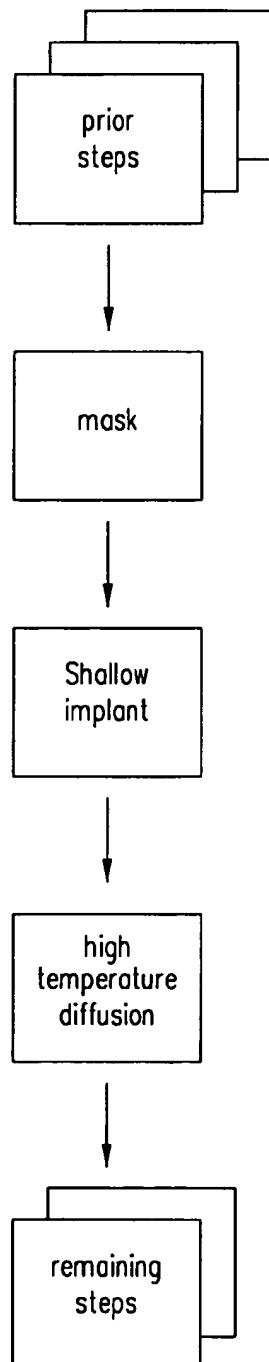


FIG. 17A
(Prior Art)

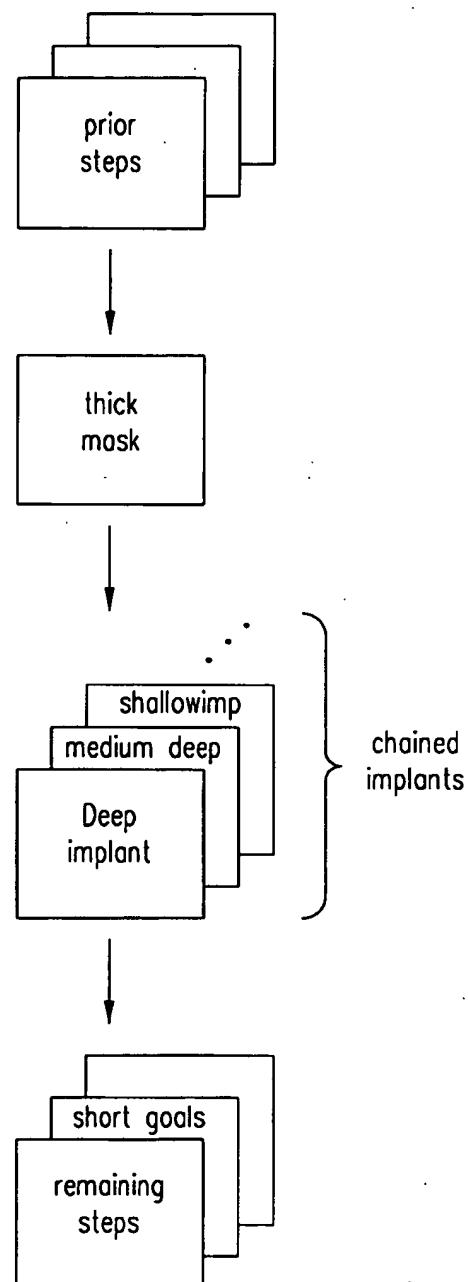


FIG. 17B

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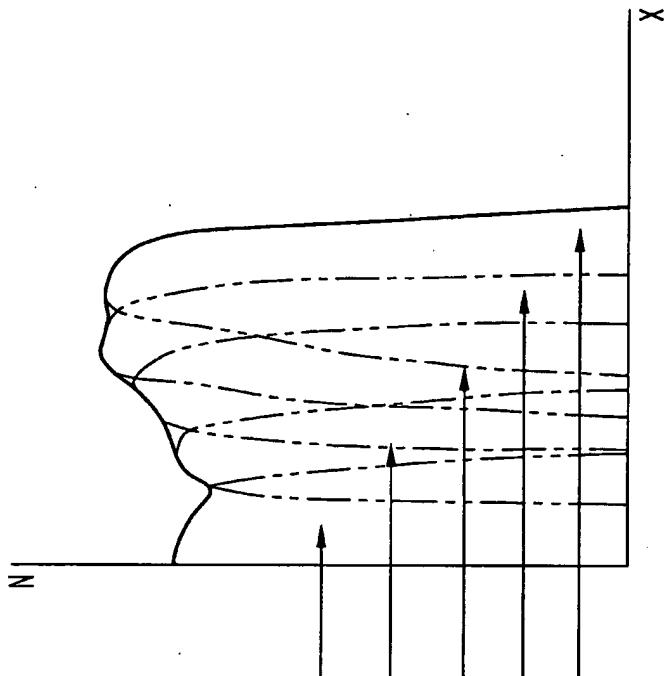


FIG. 17D

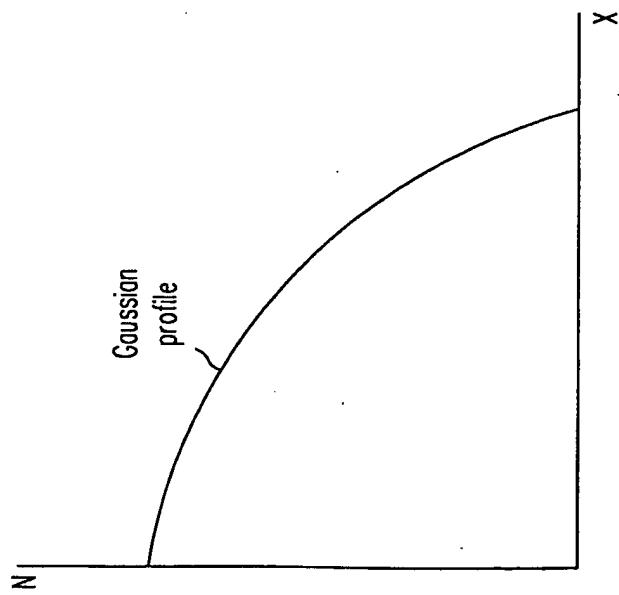


FIG. 17C
(Prior Art)

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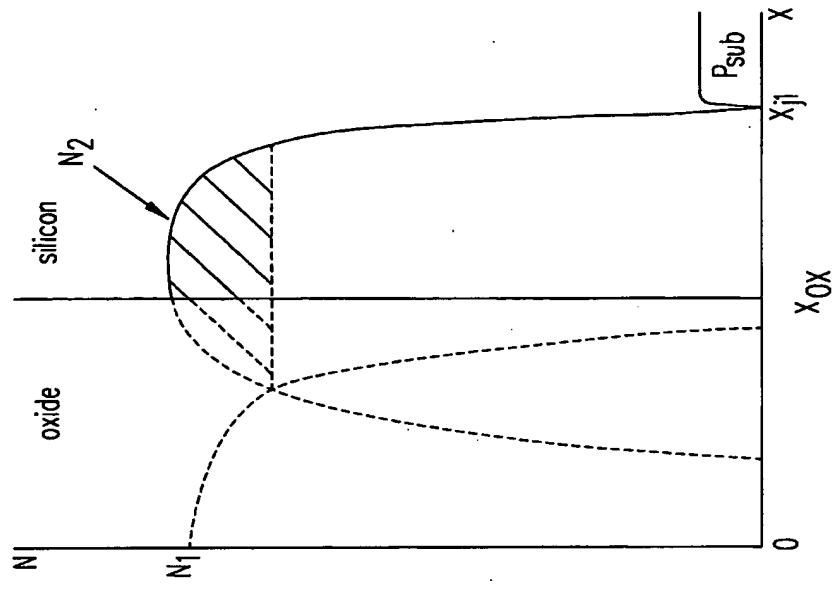


FIG. 17F

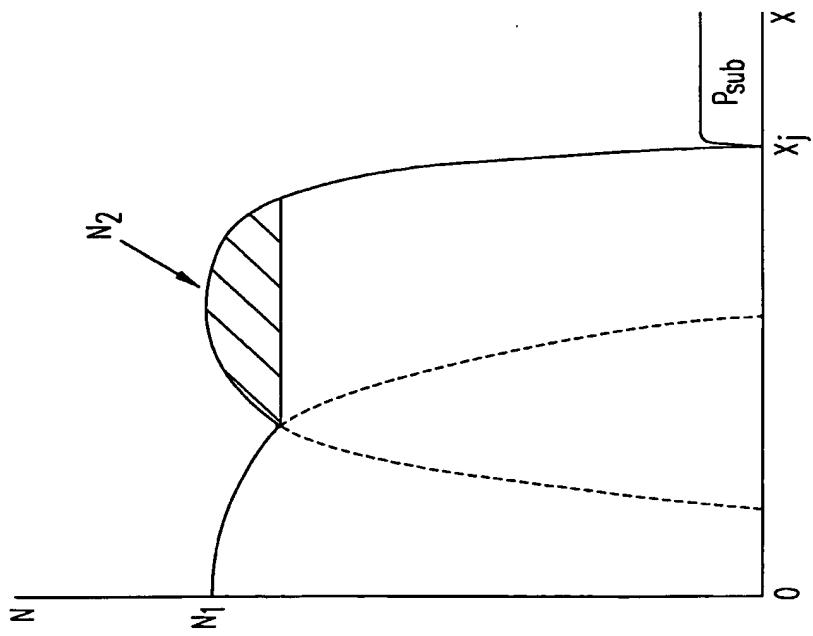


FIG. 17E

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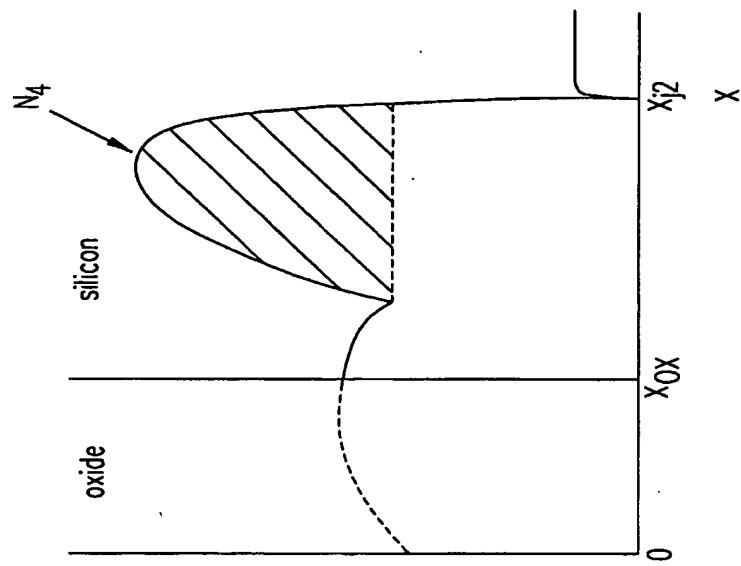


FIG. 17H

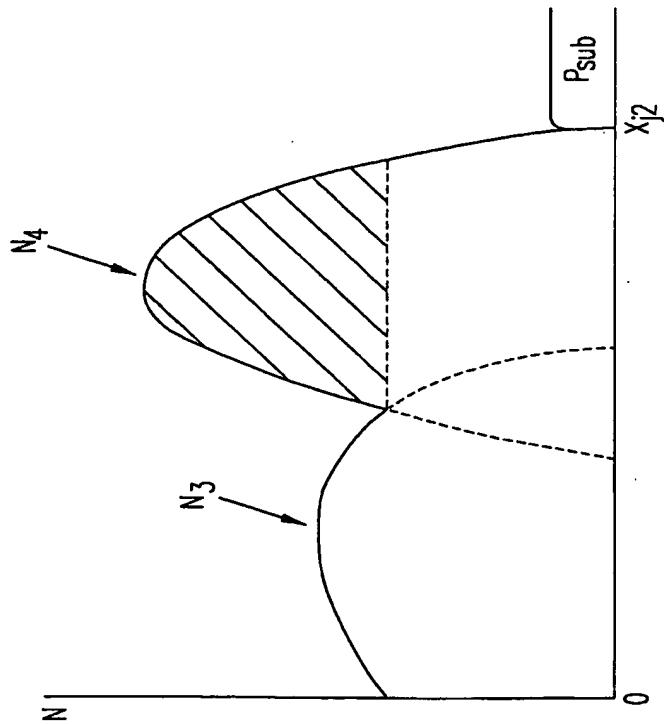


FIG. 17G

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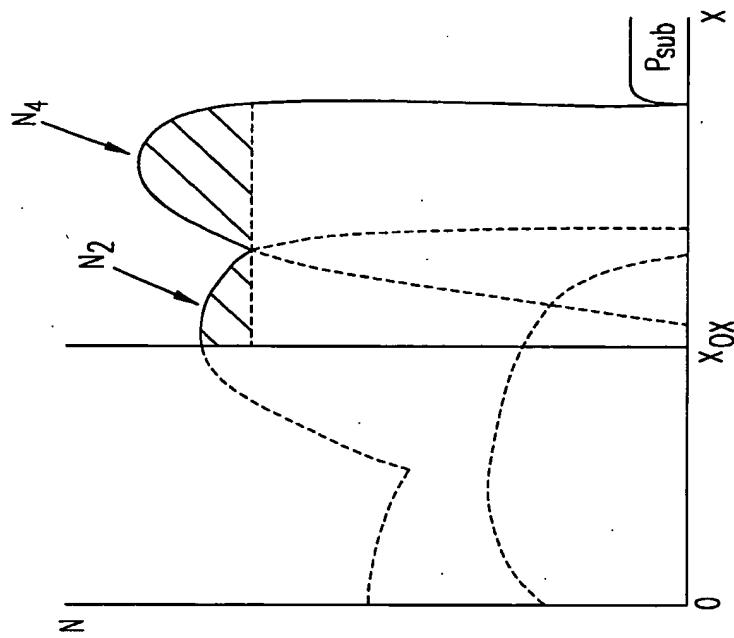


FIG. 17J

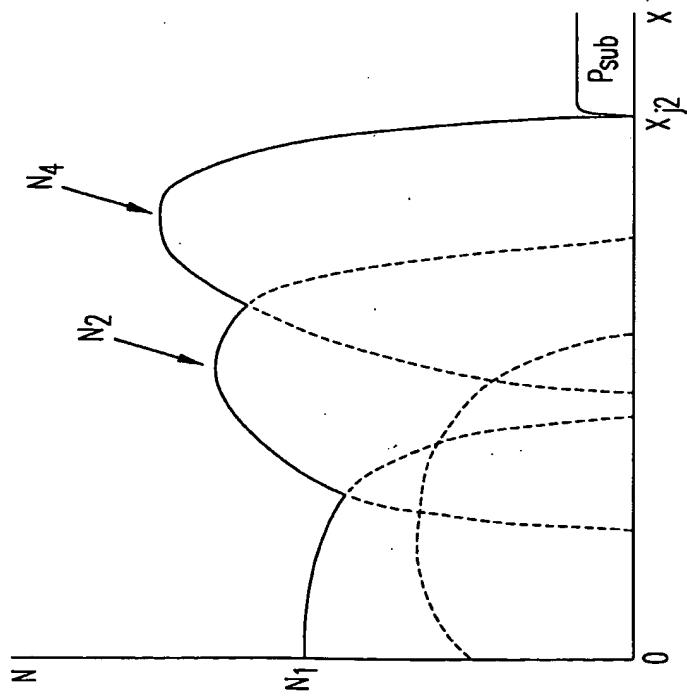


FIG. 17I

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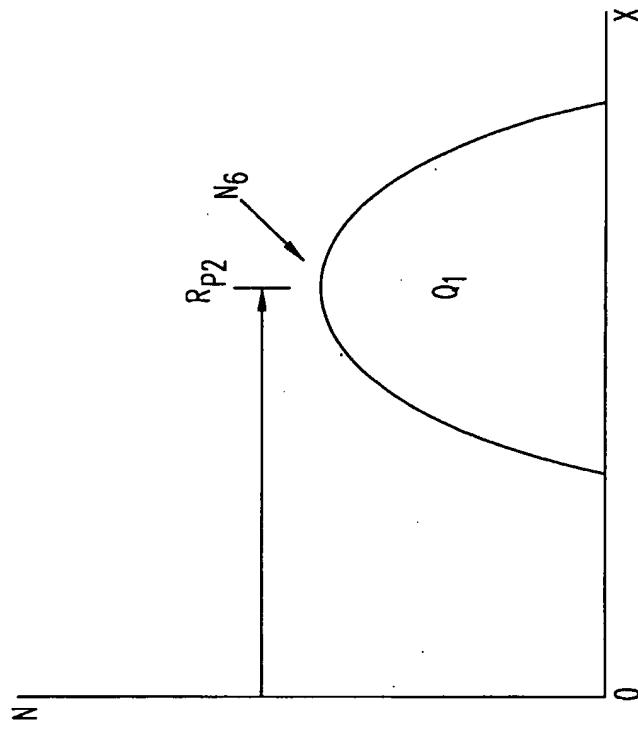


FIG. 17L
(Prior Art)

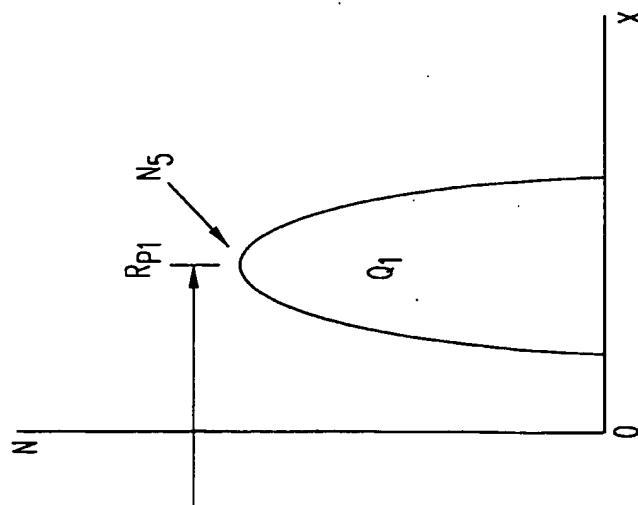


FIG. 17K
(Prior Art)

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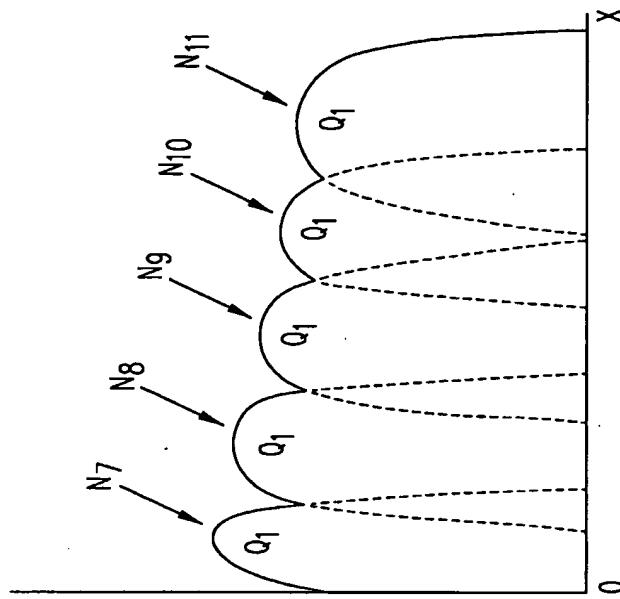


FIG. 17N

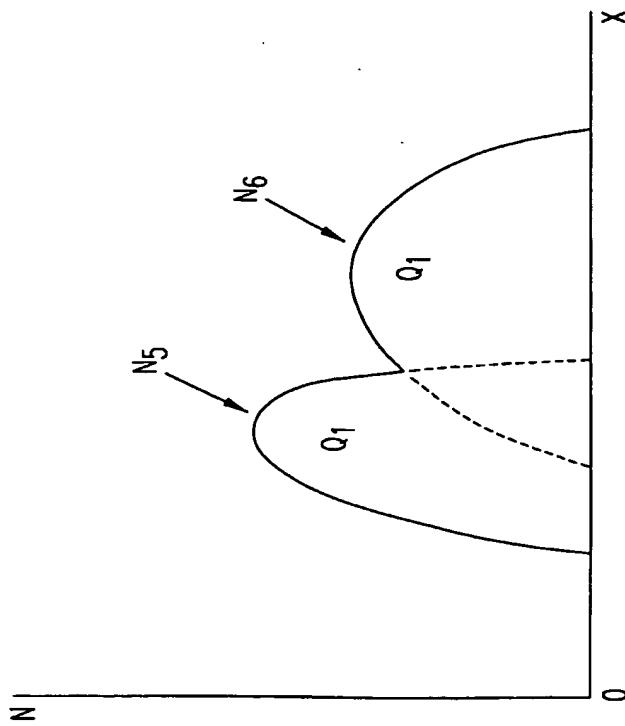


FIG. 17M

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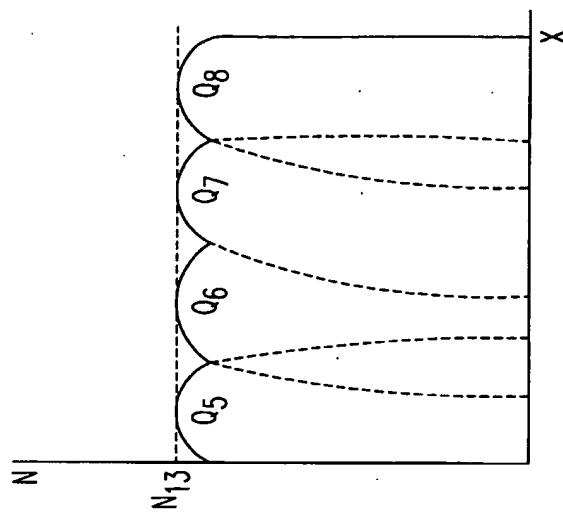


FIG. 17P

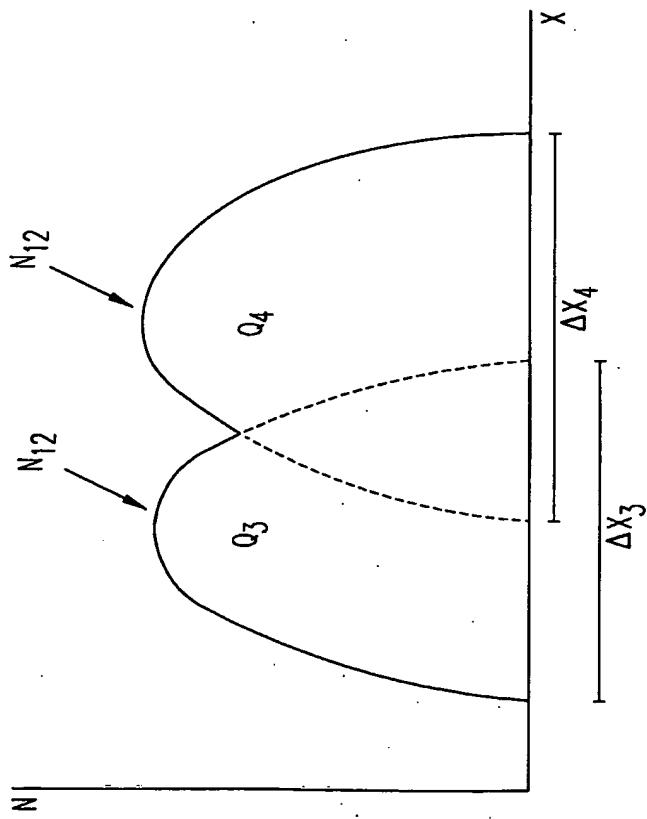


FIG. 17O

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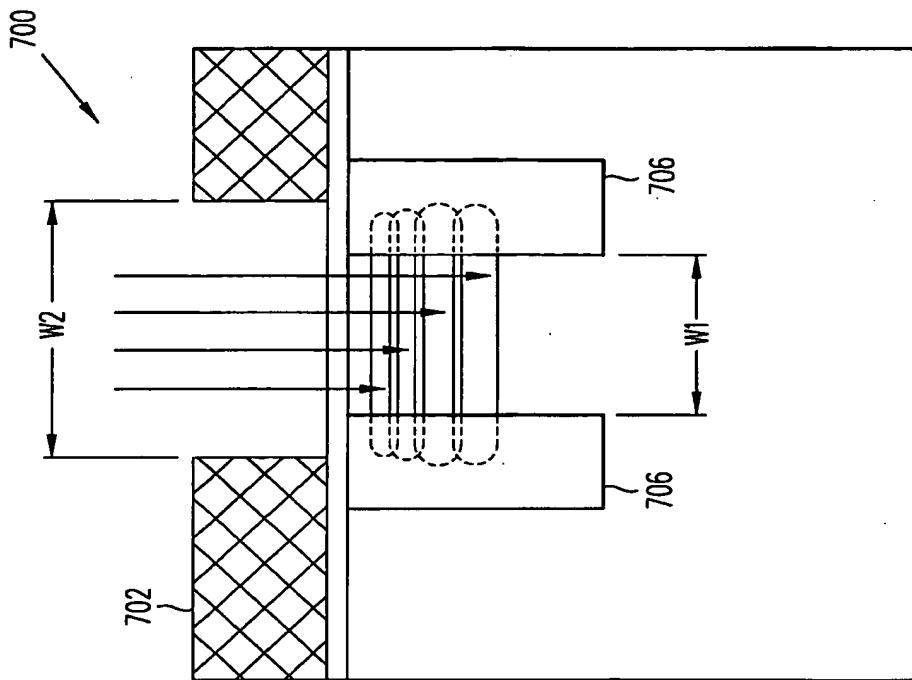


FIG. 17R

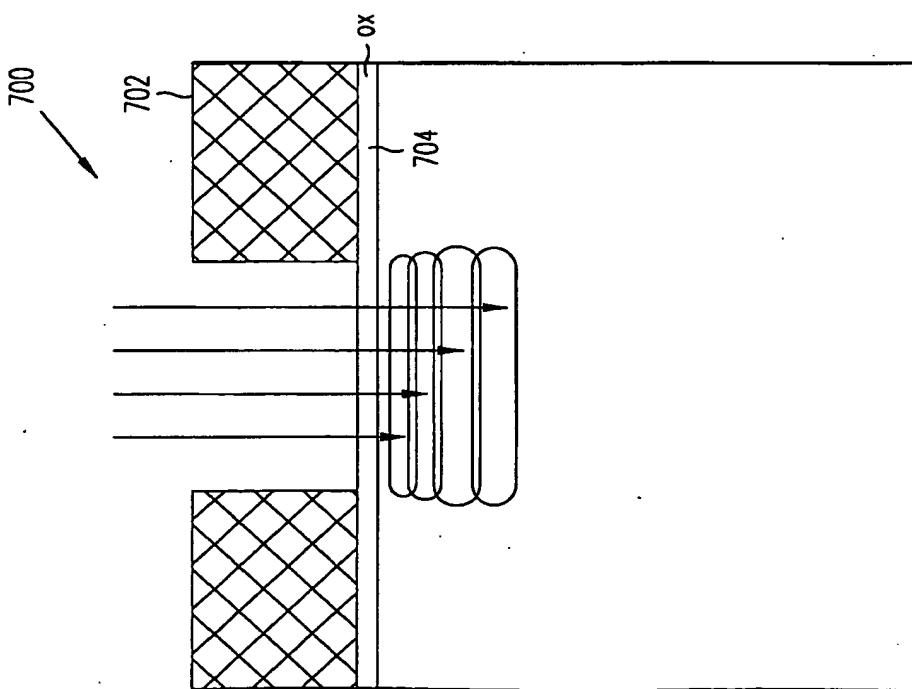


FIG. 17Q

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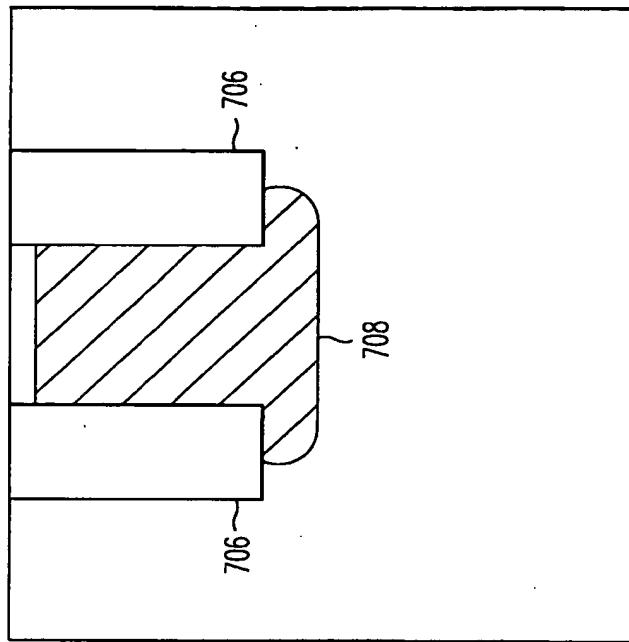


FIG. 17T

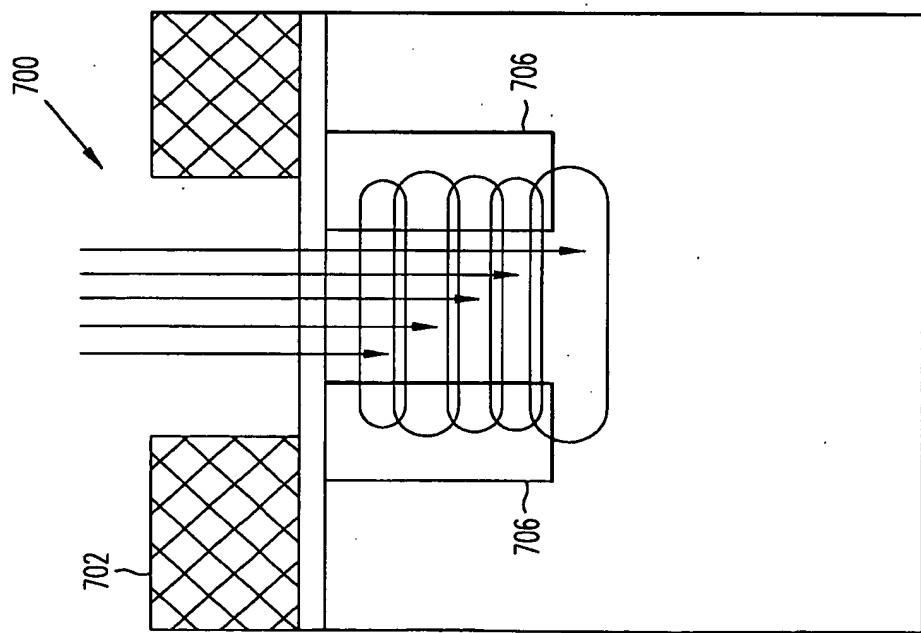


FIG. 17S

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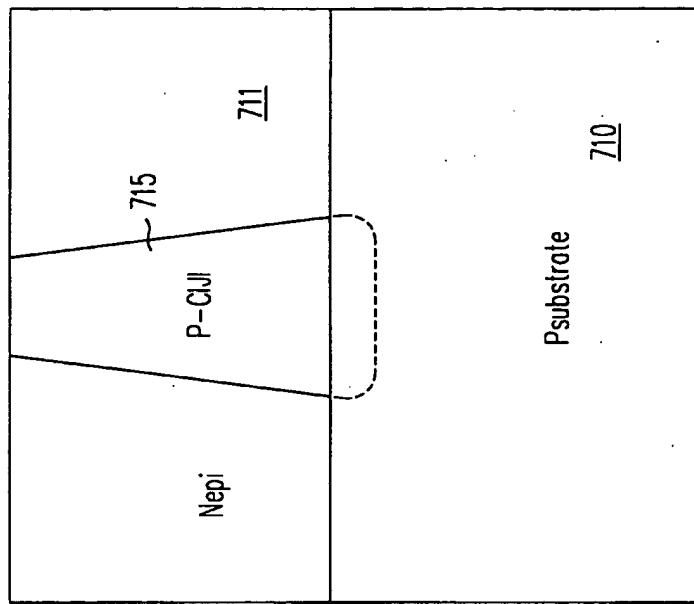


FIG. 17V

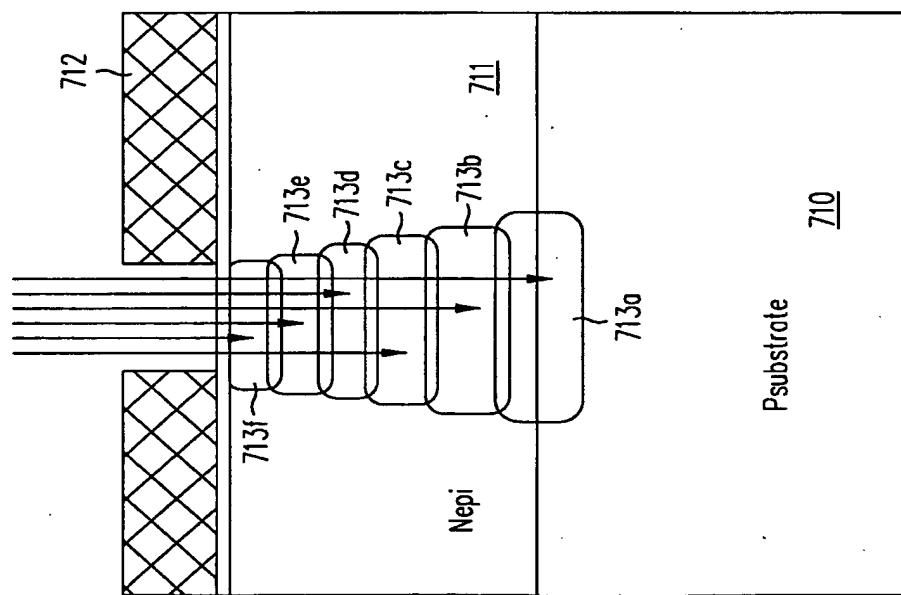


FIG. 17U

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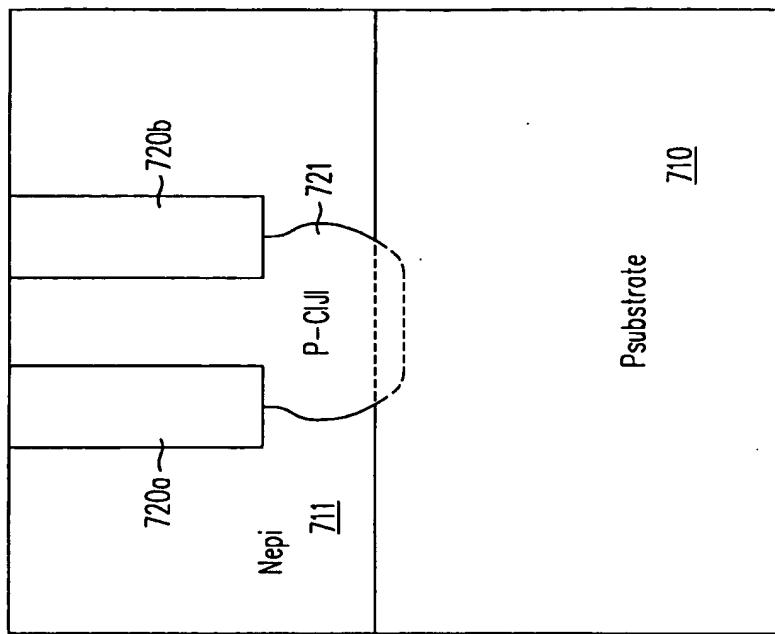


FIG. 17X

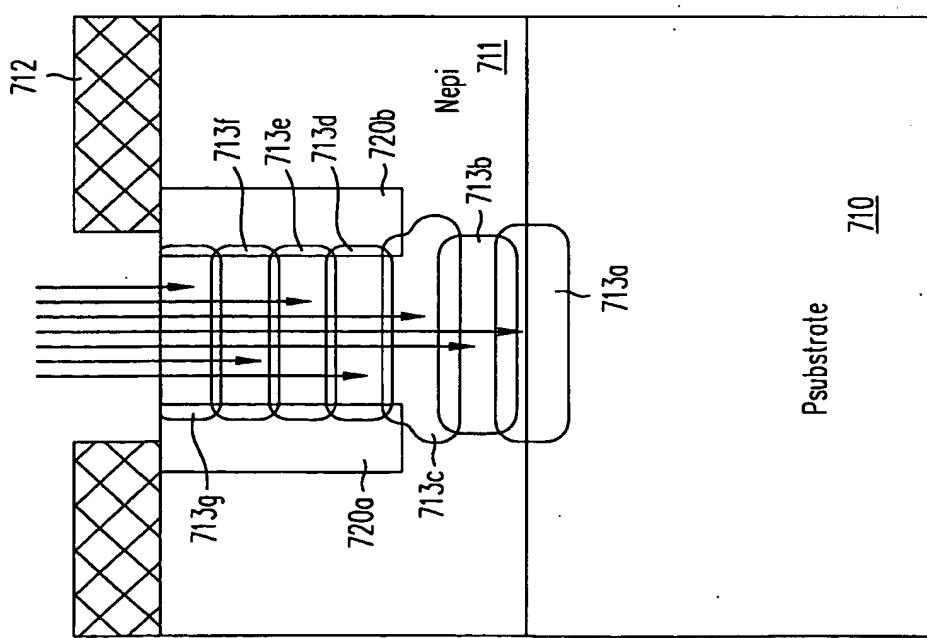


FIG. 17W

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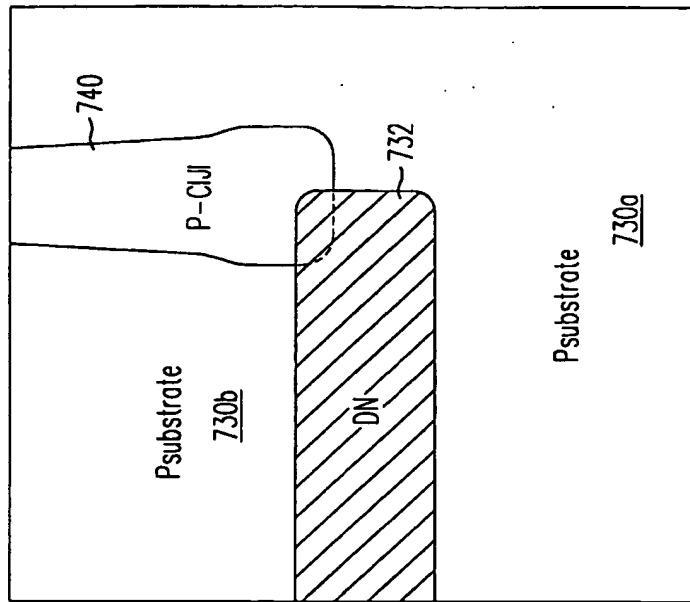


FIG. 17Z

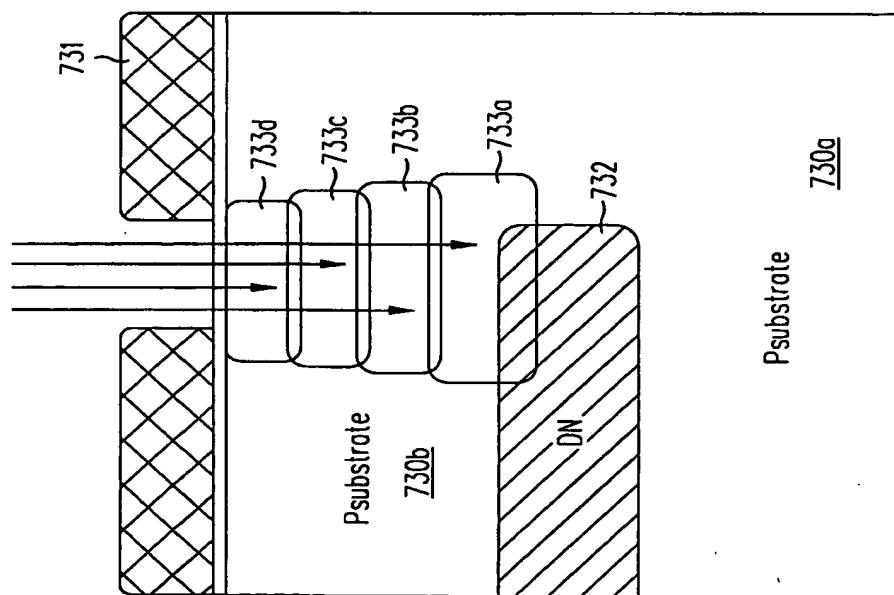


FIG. 17Y

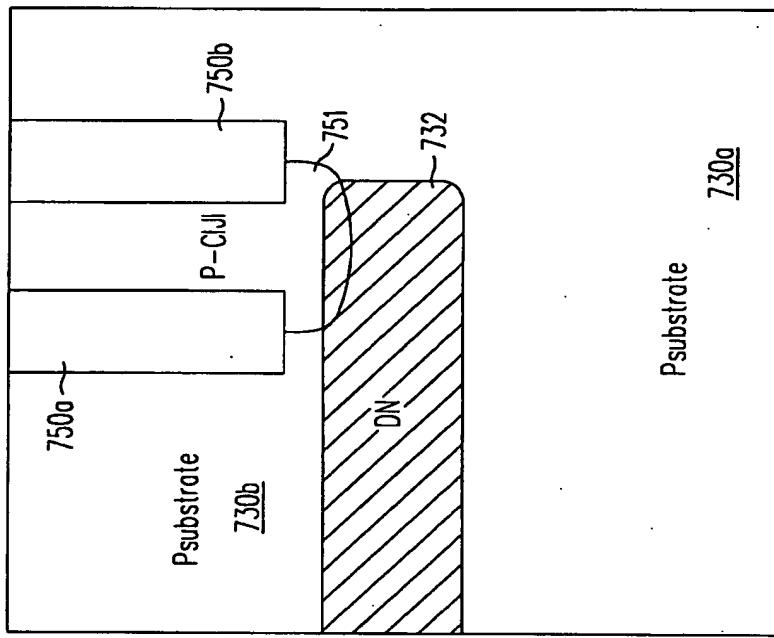


FIG. 17BB

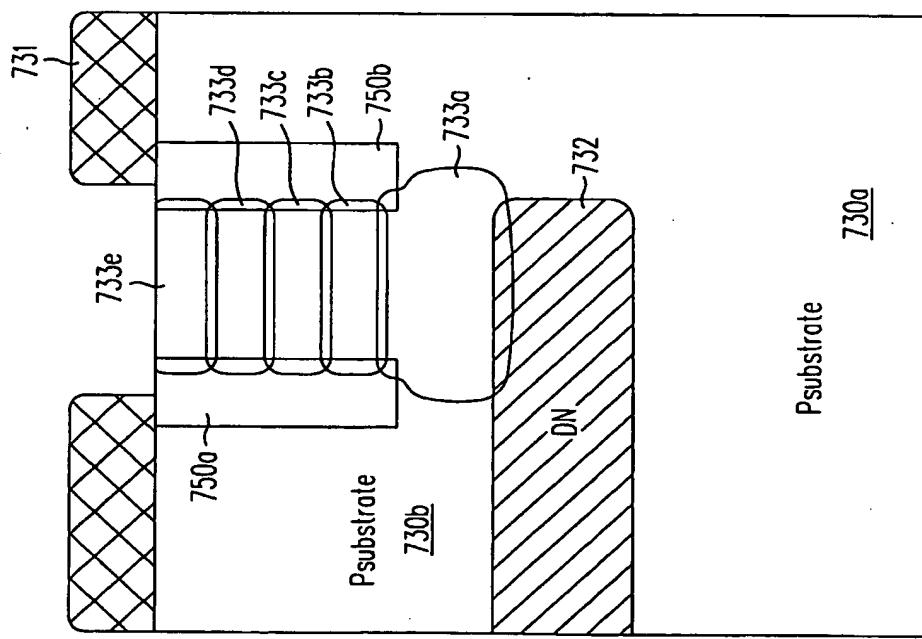


FIG. 17AA

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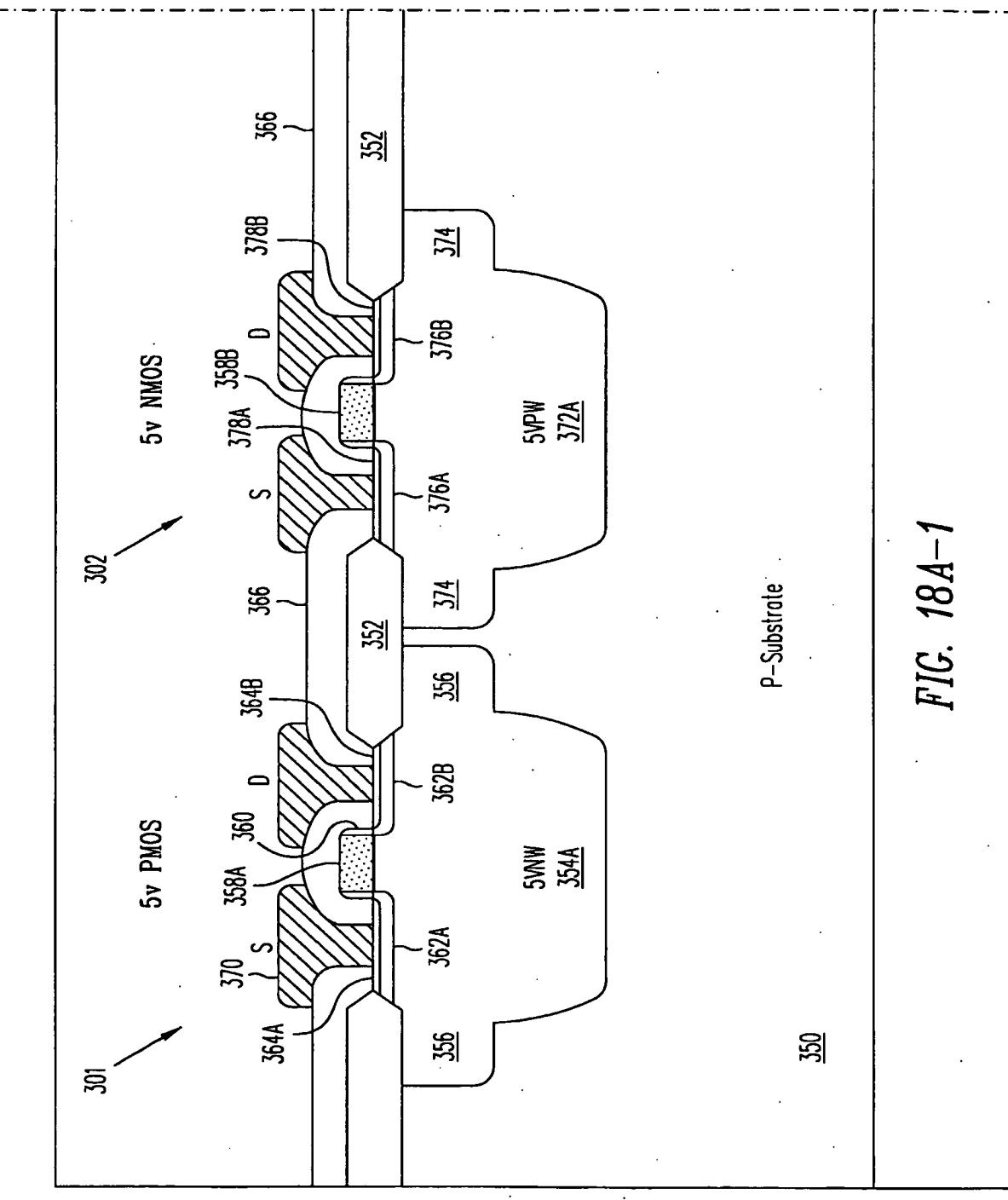


FIG. 18A-1 FIG. 18A-2	FIG. 18A-3 FIG. 18A-4
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Key To

FIG. 18A

FIG. 18A-1

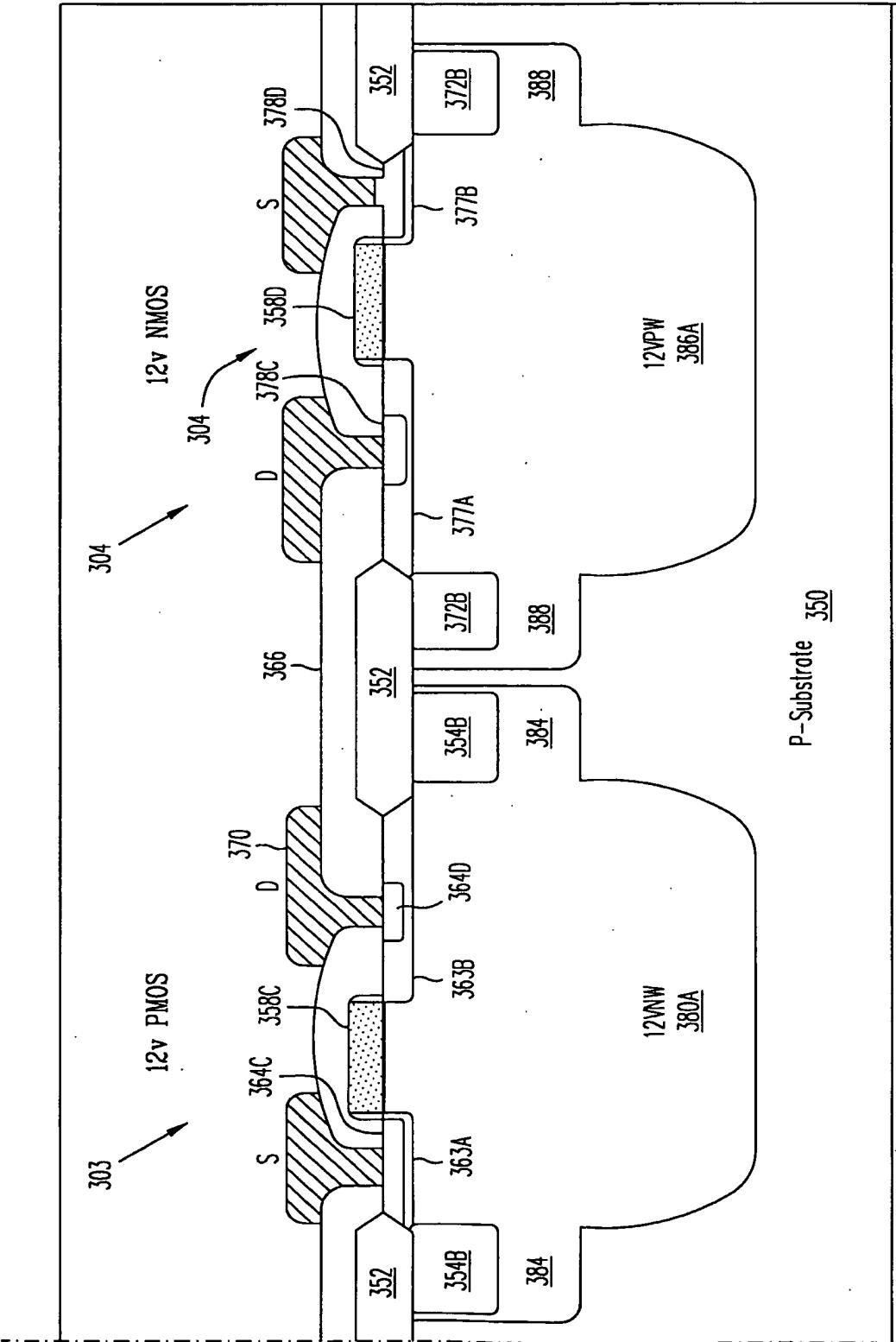


FIG. 18A-2

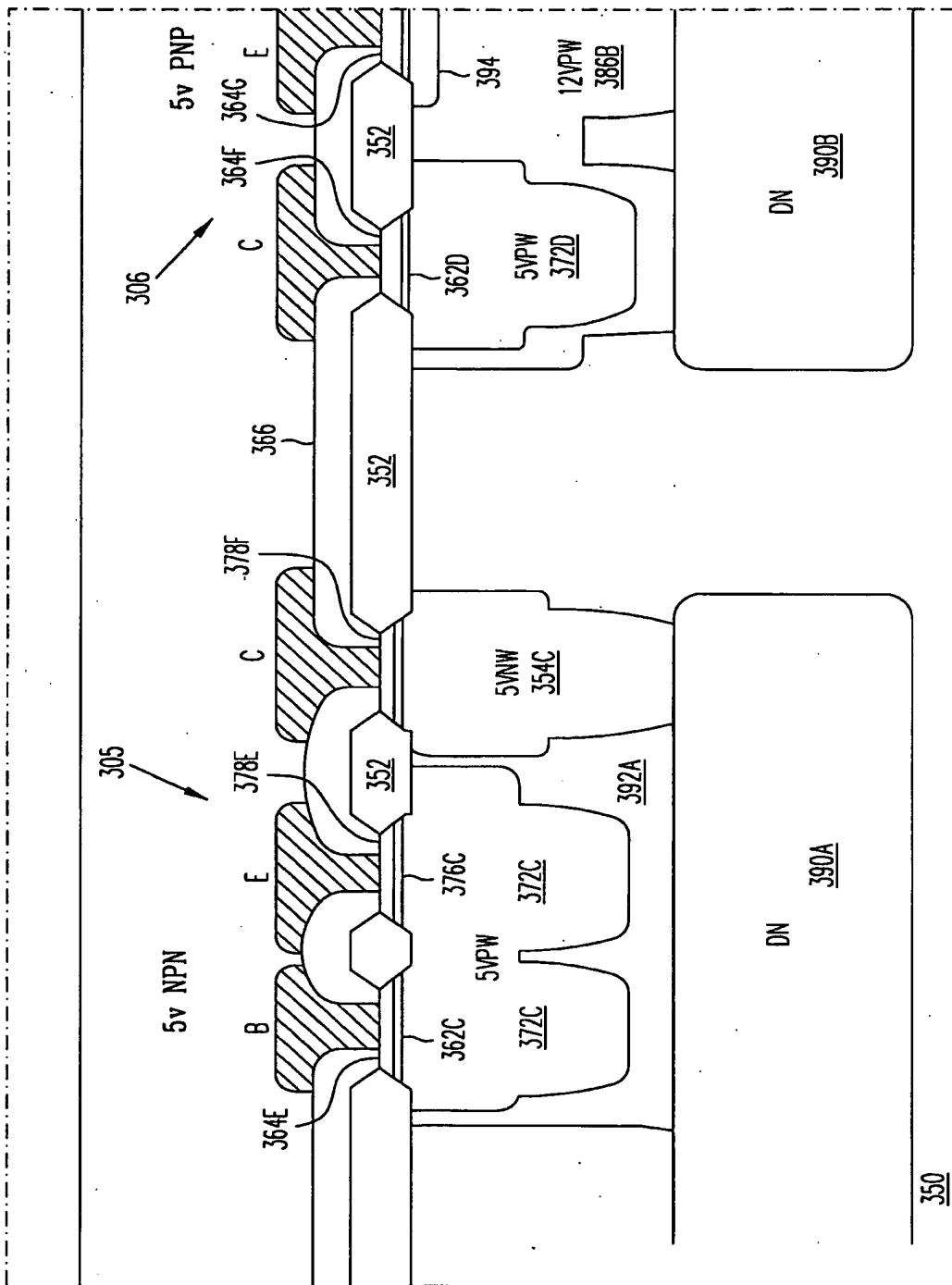


FIG. 18A-3

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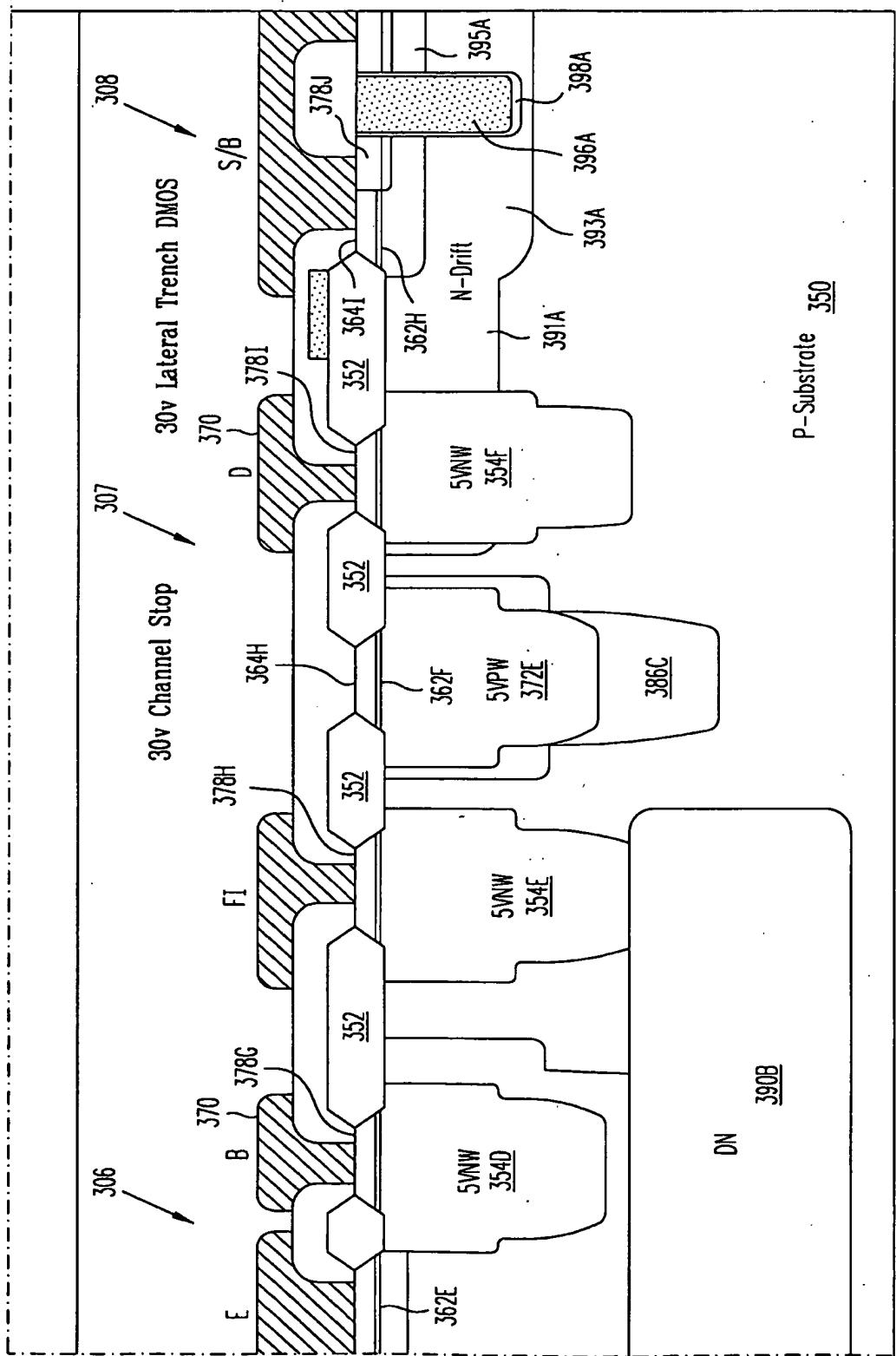
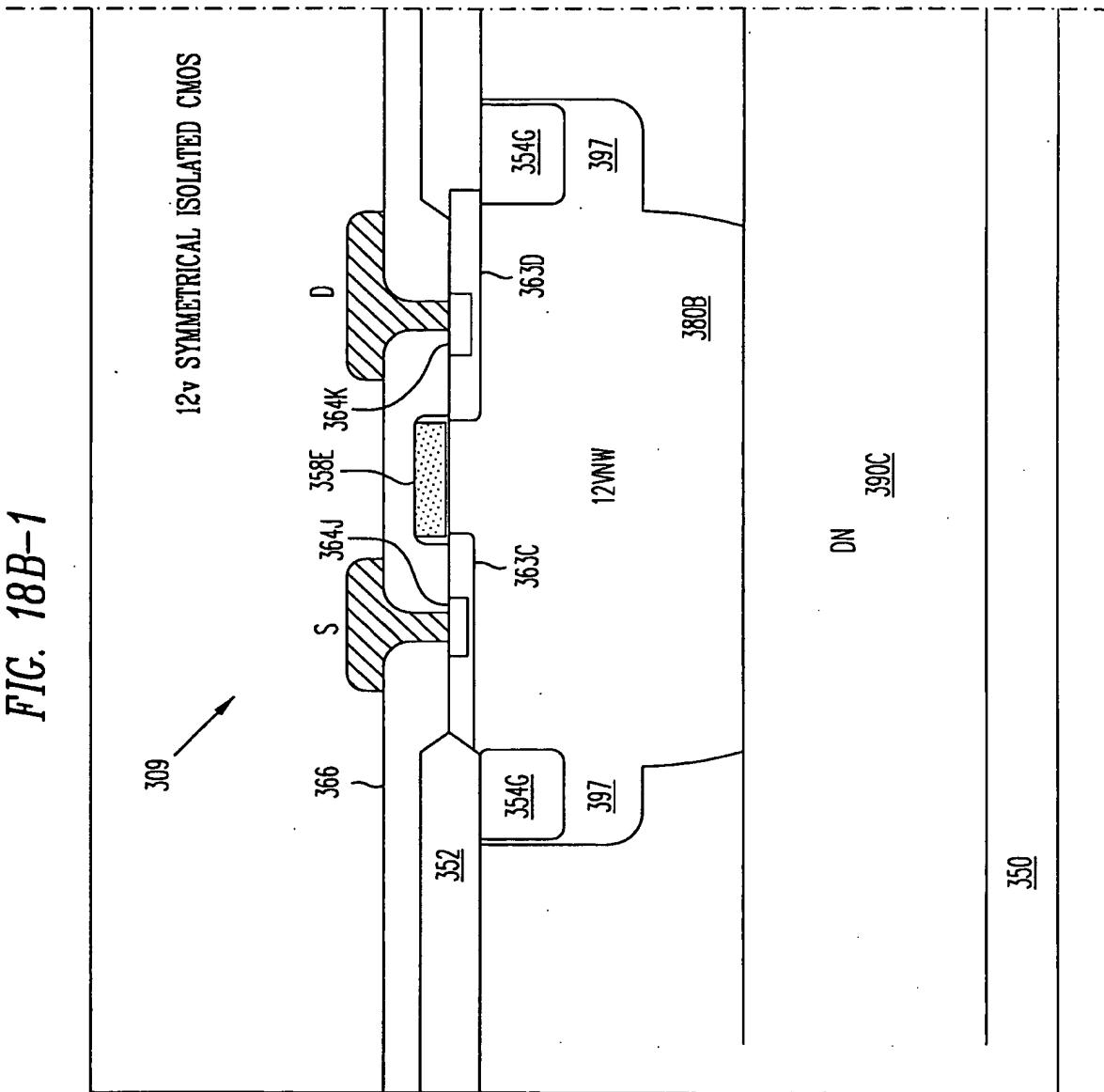


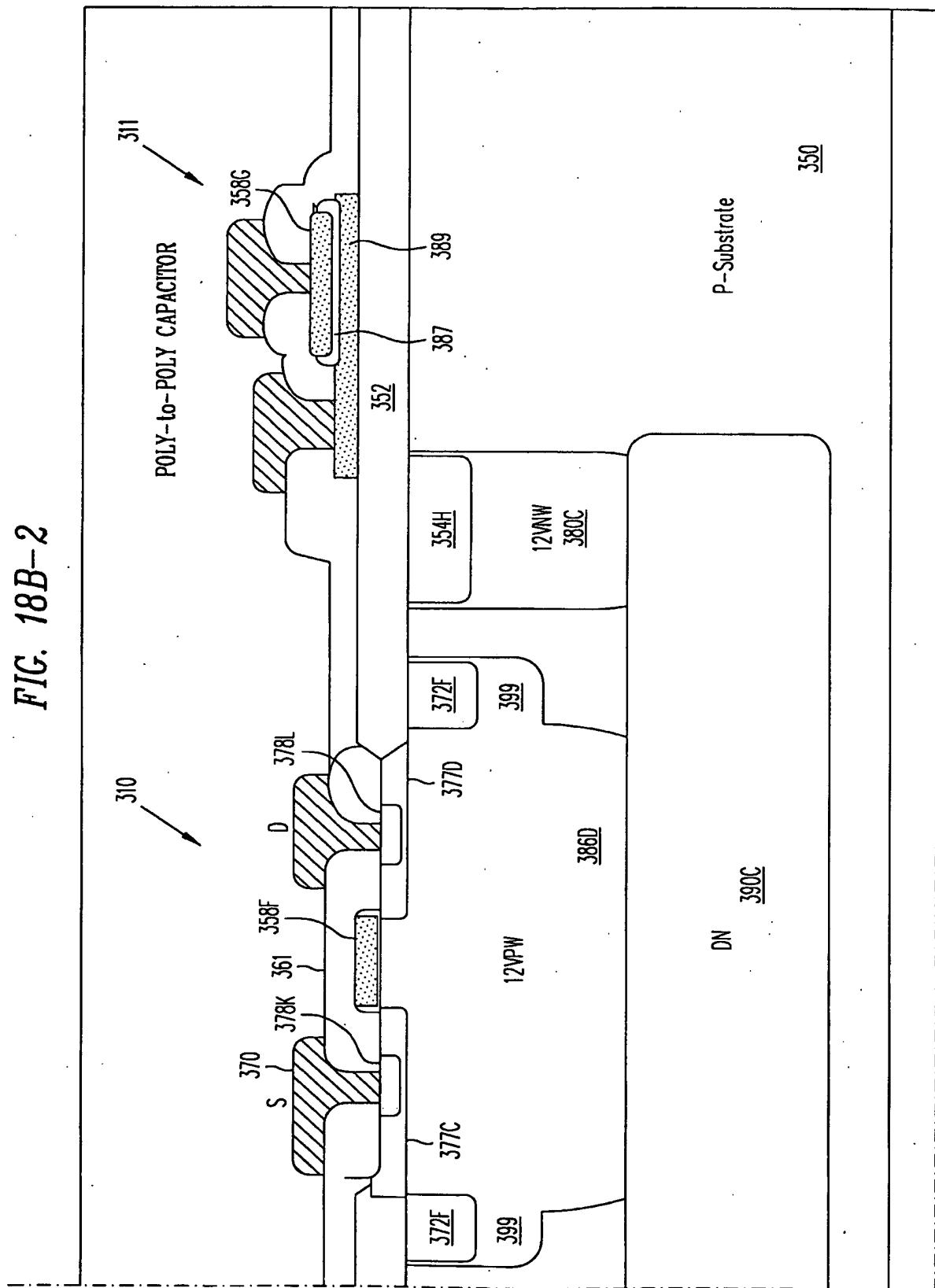
FIG. 18A-4

FIG. 18B-1*FIG. 18B*

Key To

<i>FIG. 18B-1</i>	<i>FIG. 18B-2</i>
<i>FIG. 18B-3</i>	<i>FIG. 18B-4</i>

FIG. 18B-2



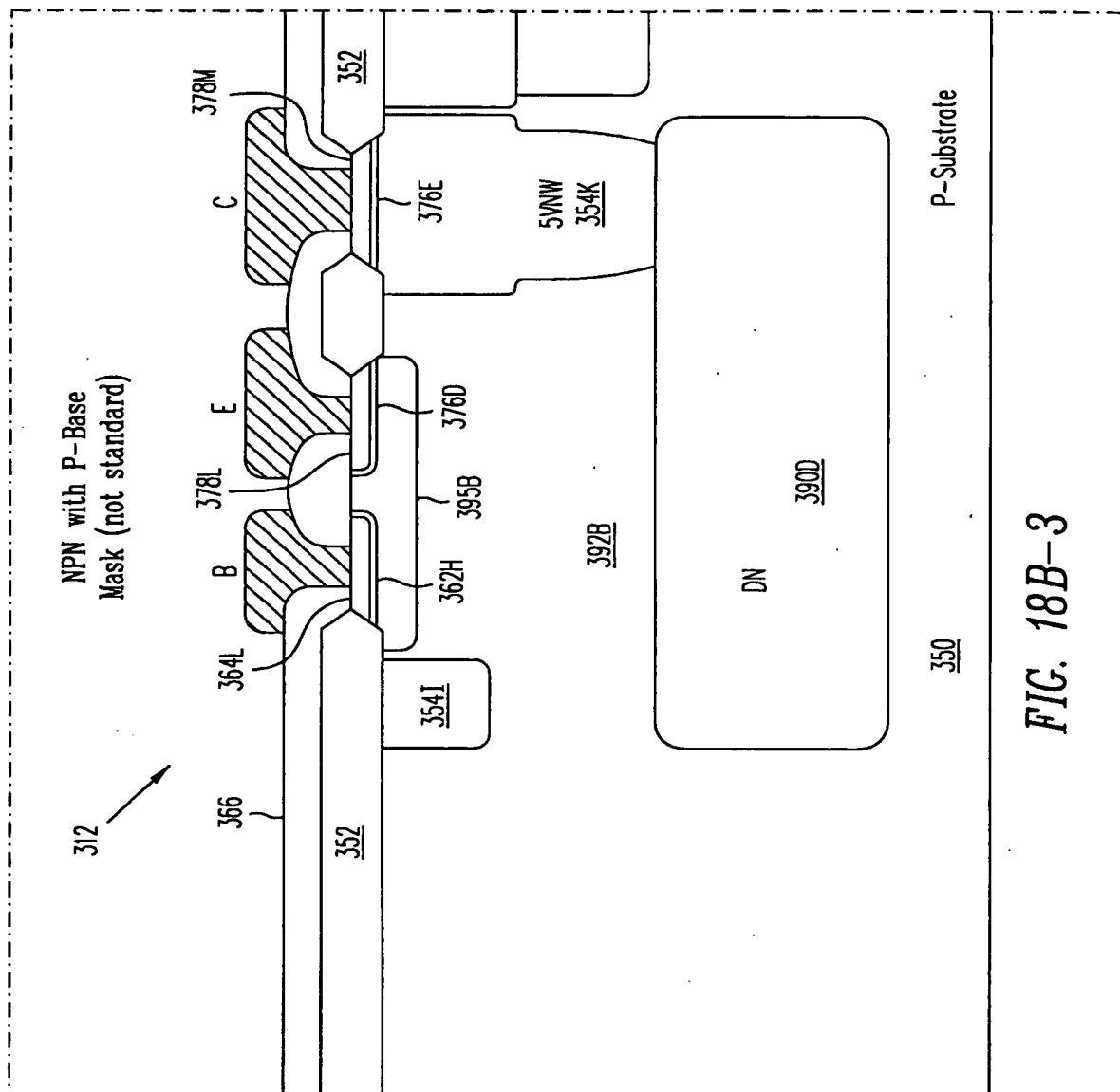


FIG. 18B-3

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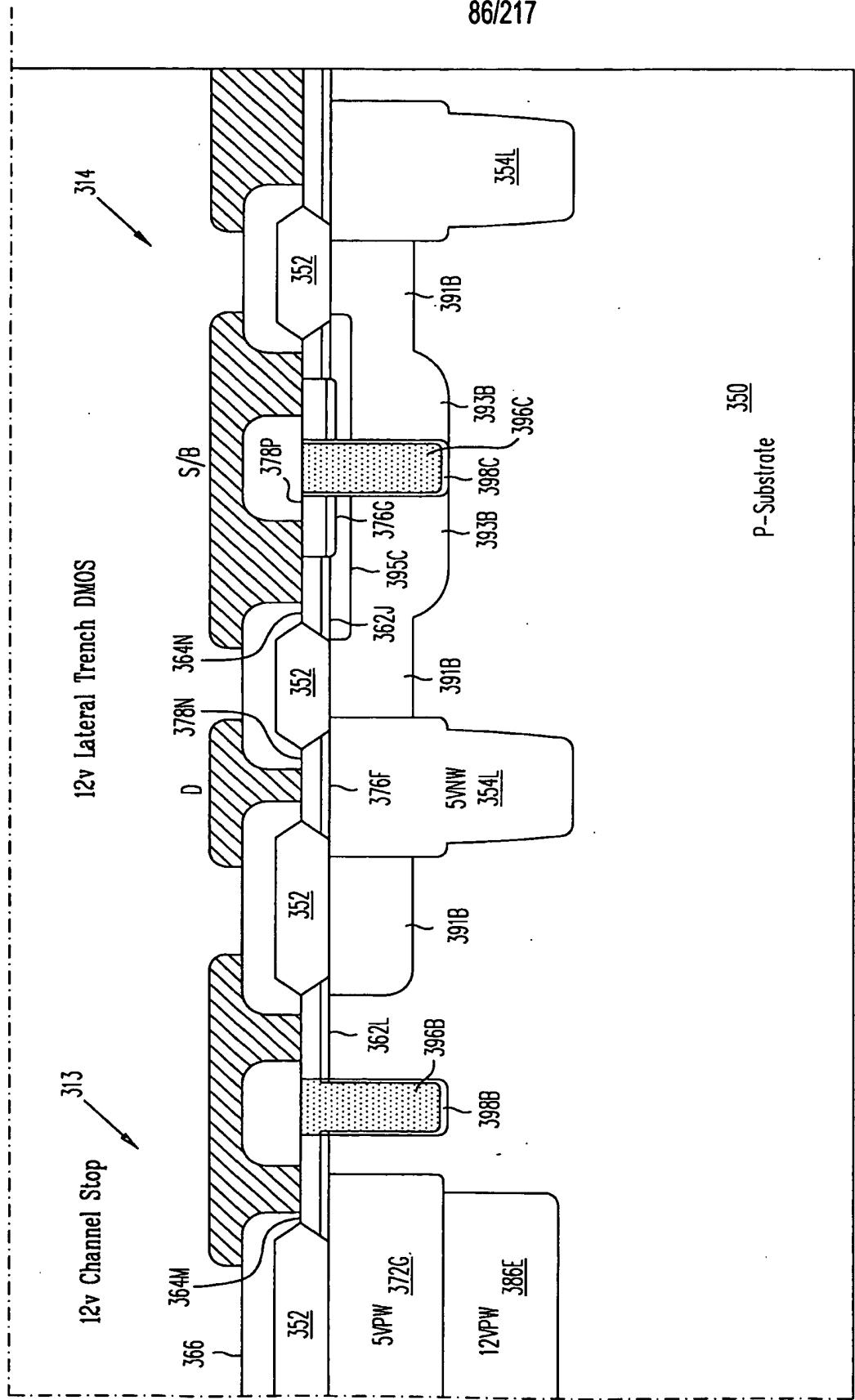


FIG. 18B-4

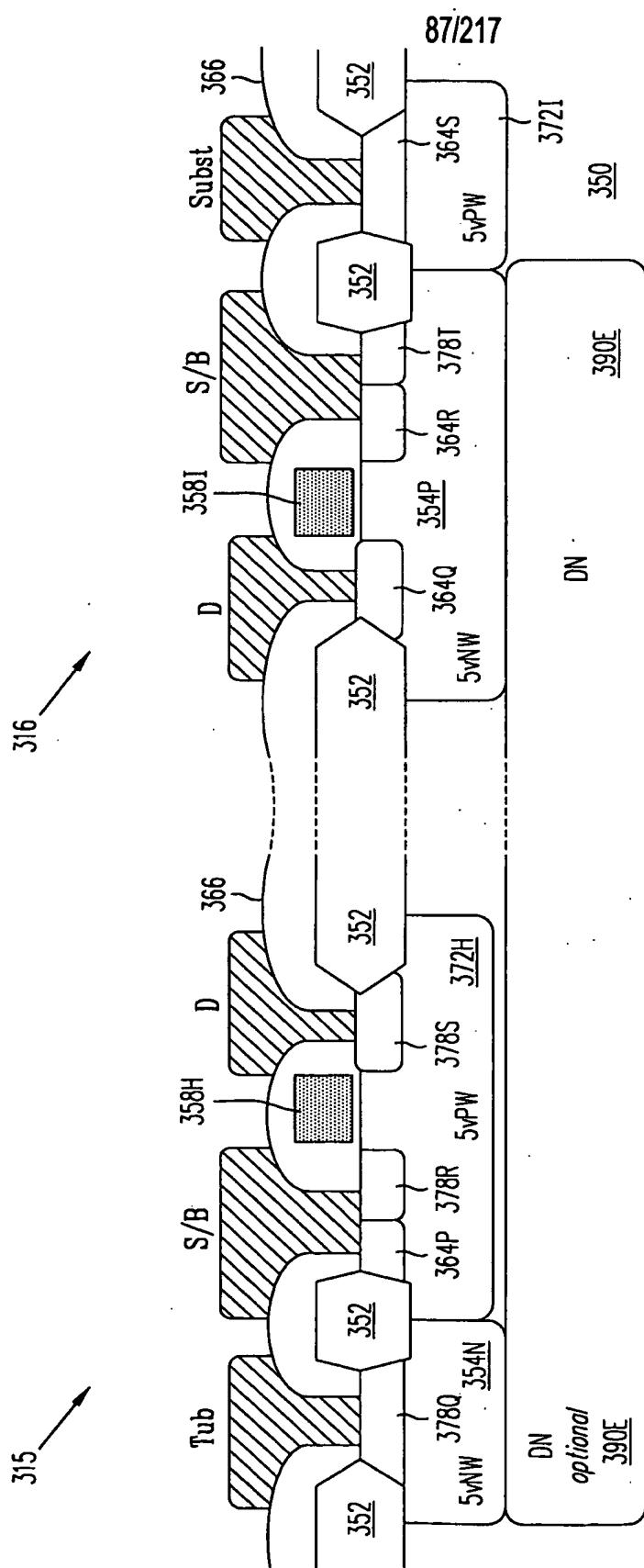


FIG. 18C

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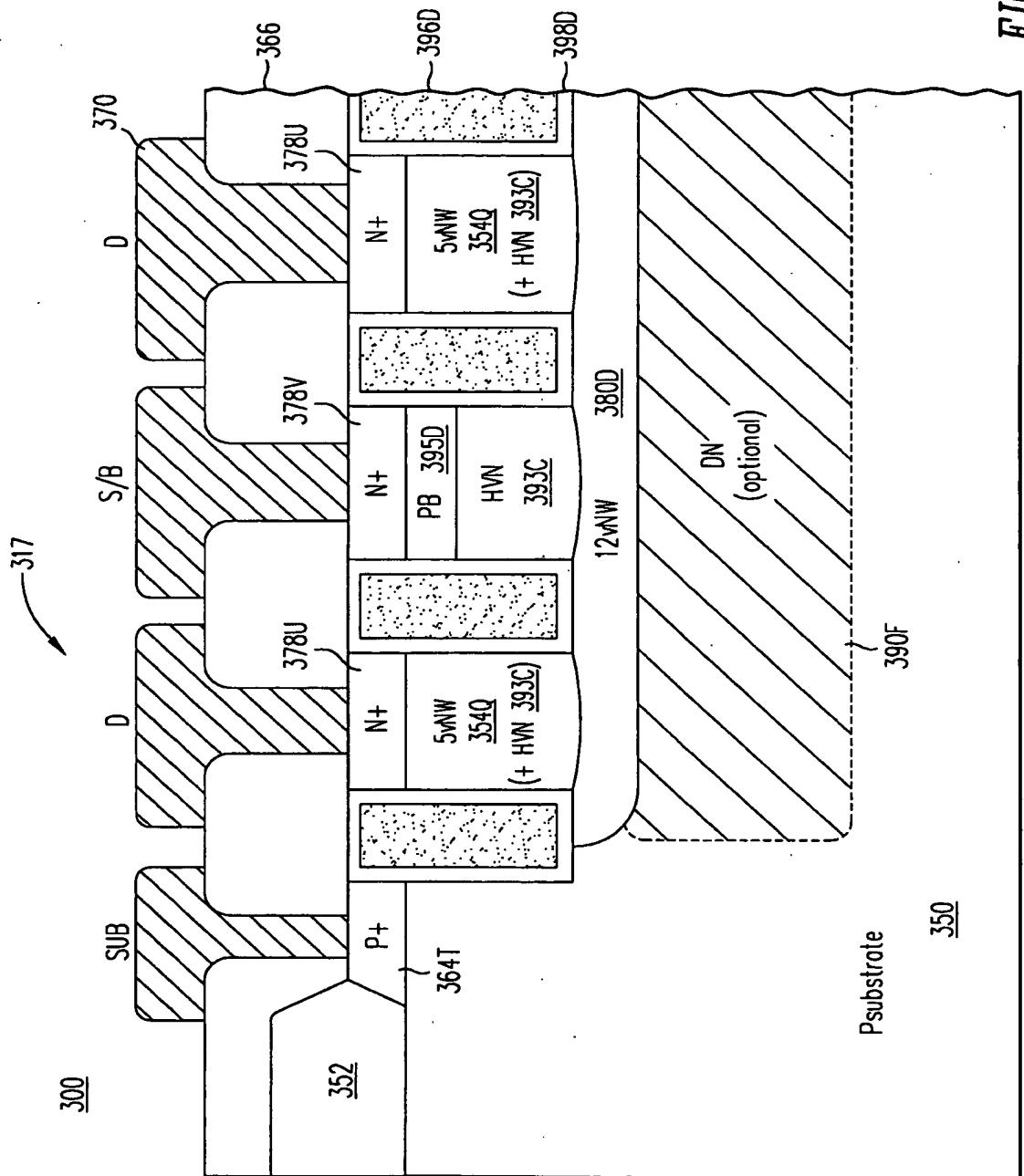
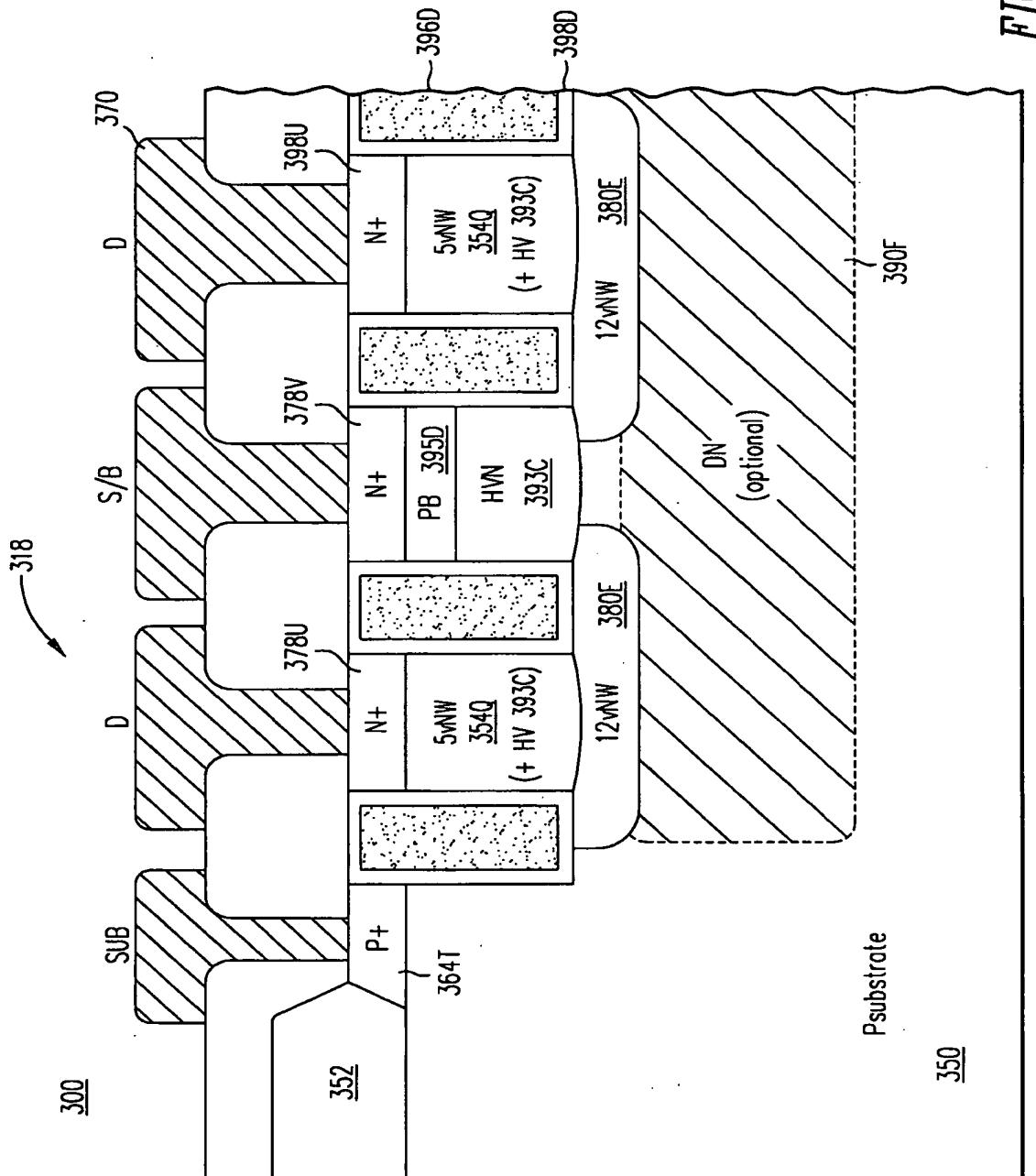


FIG. 18D



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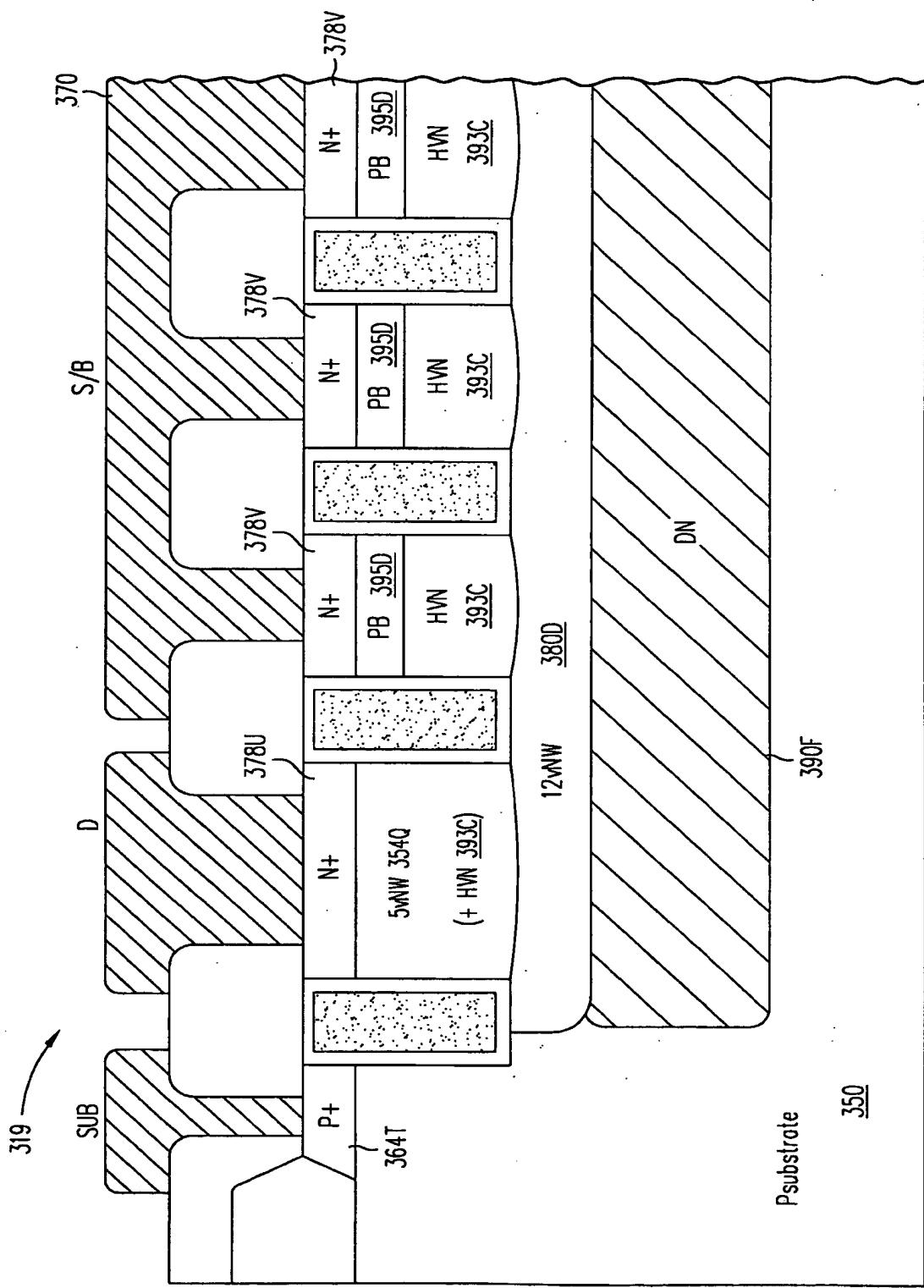


FIG. 18F

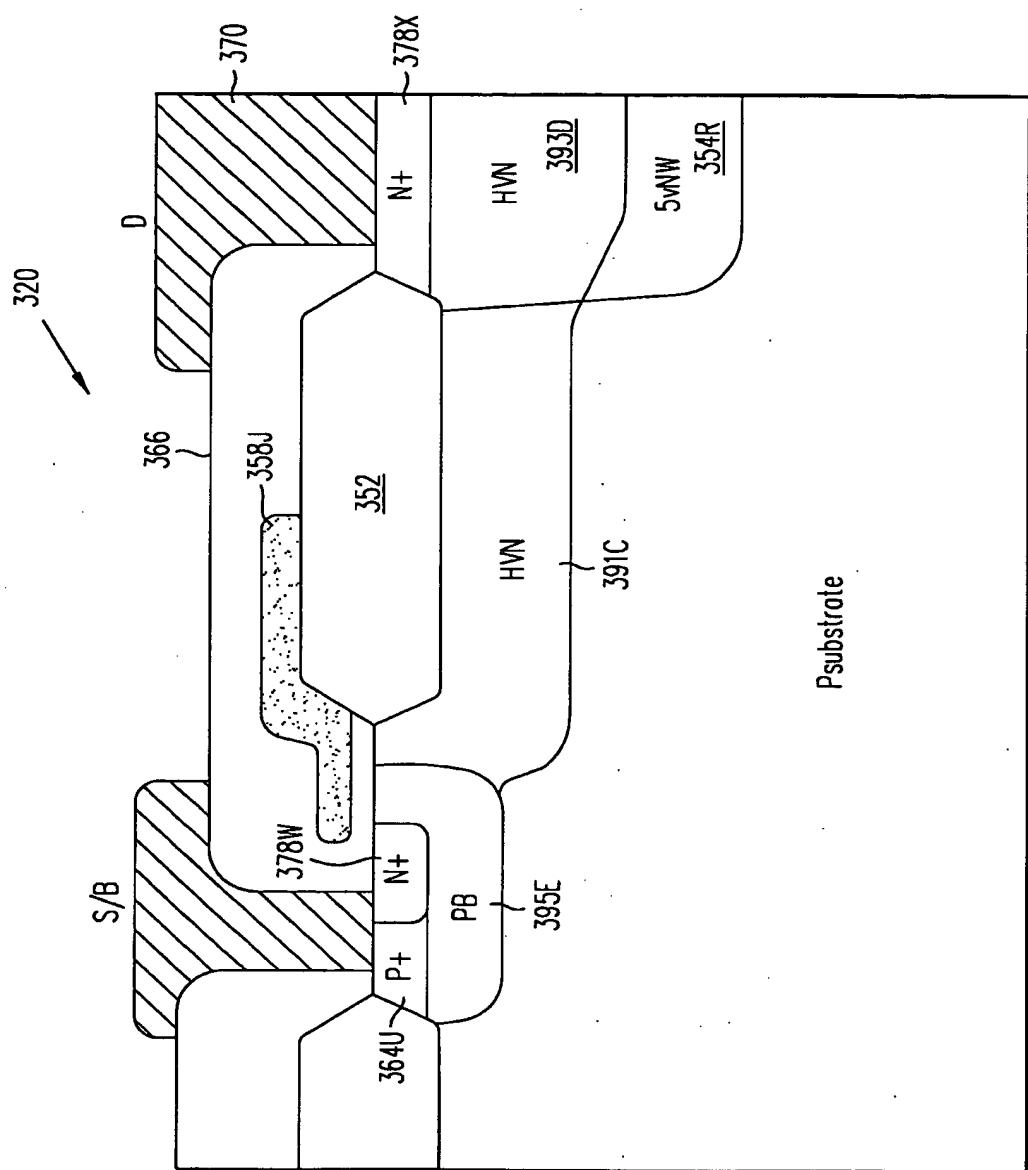


FIG. 18G

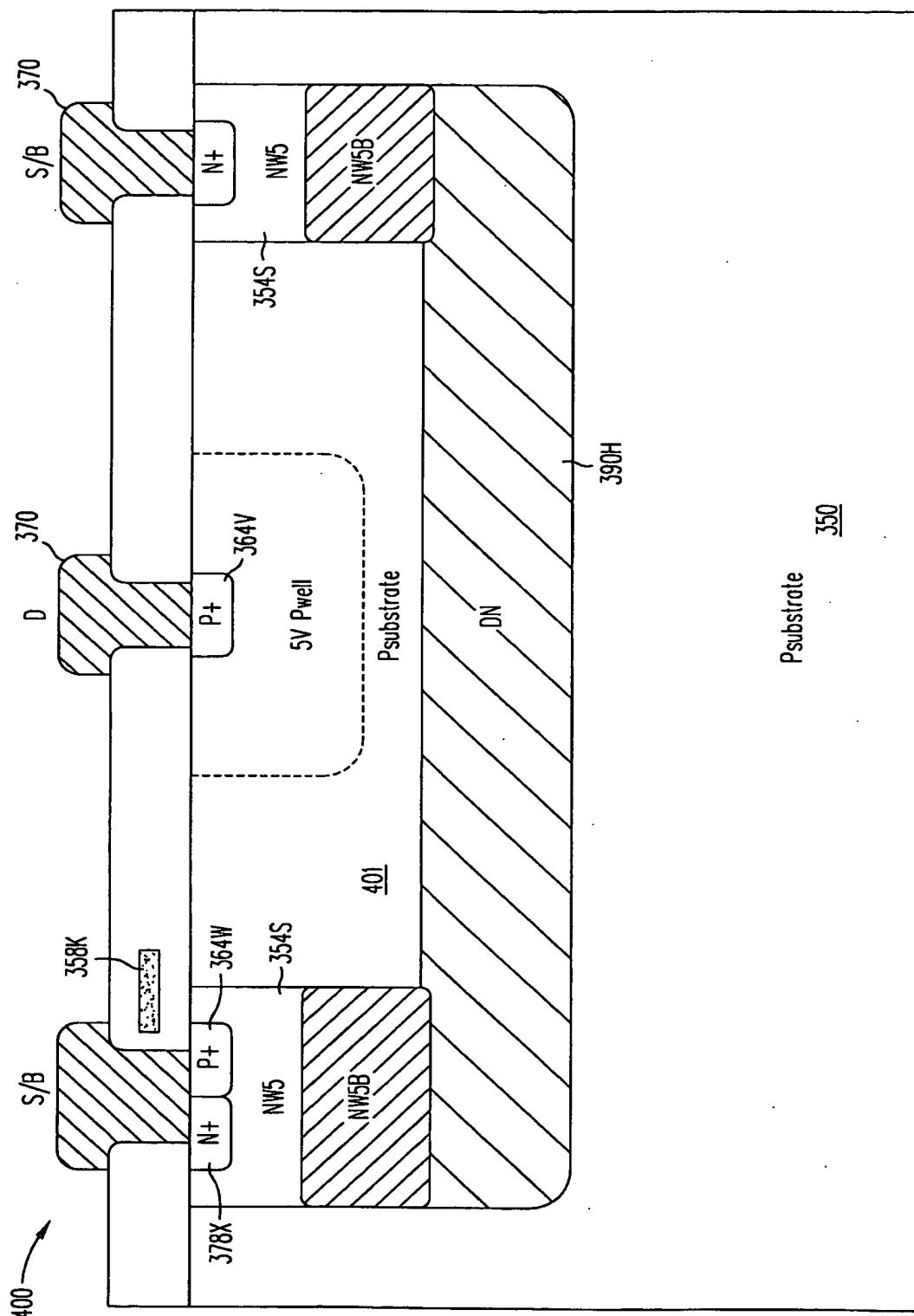


FIG. 18H

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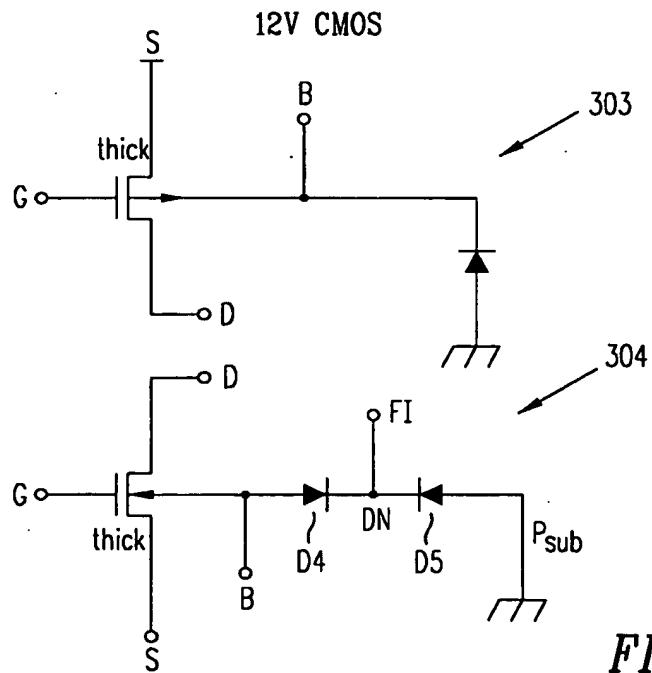
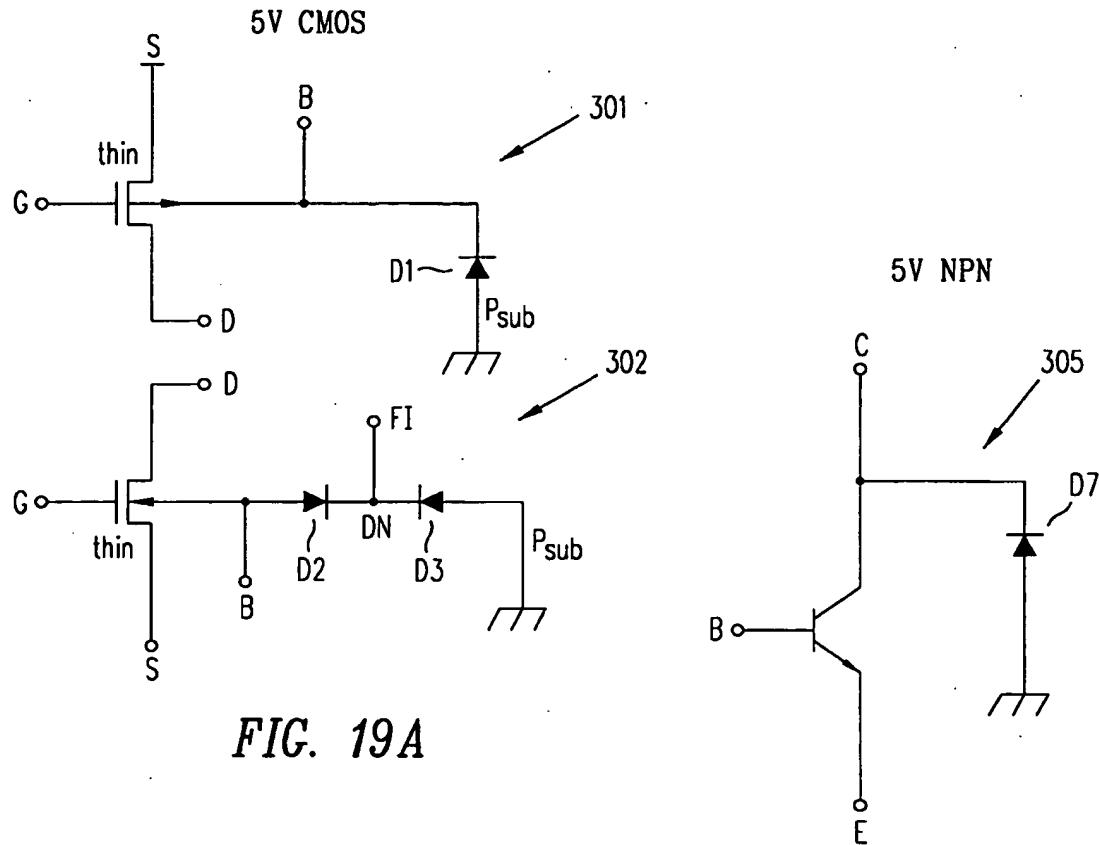


FIG. 19C

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5V PNP

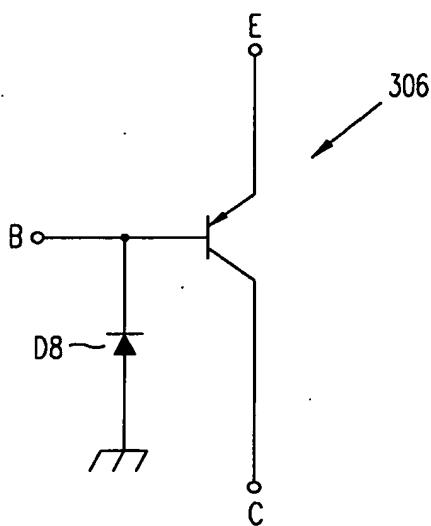


FIG. 19D

30V Trench
LDMOS

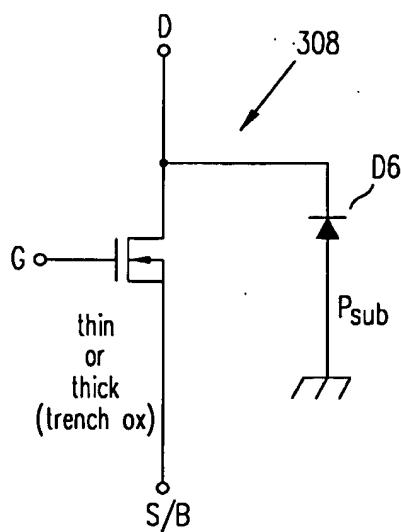


FIG. 19E

30V LDMOS

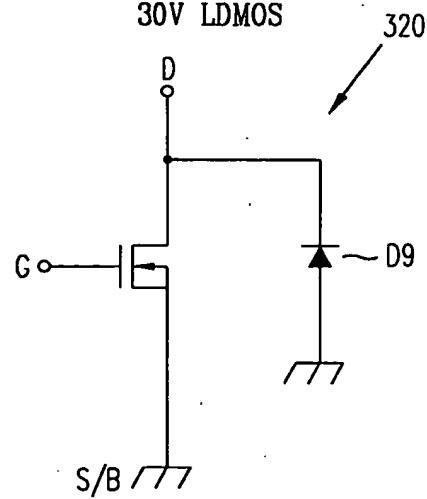


FIG. 19F

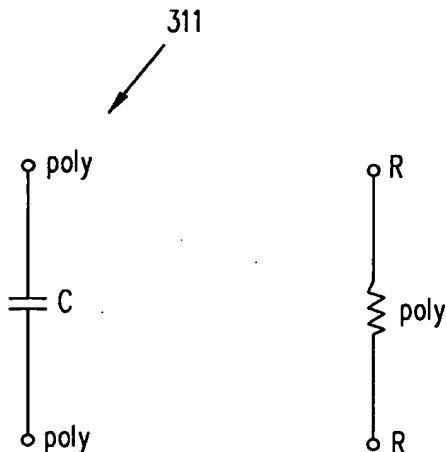
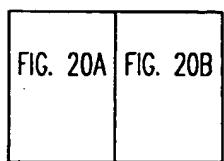
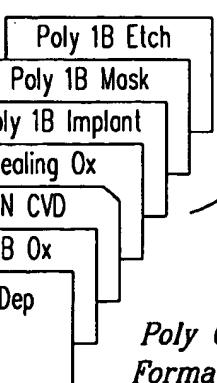
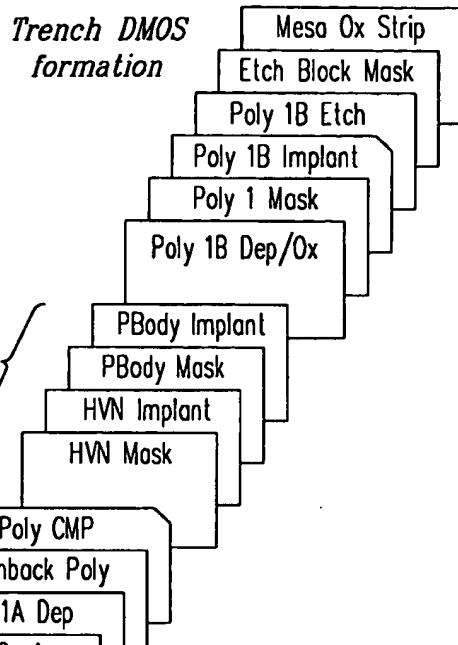
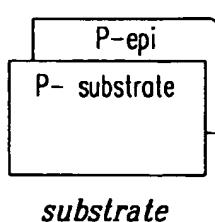
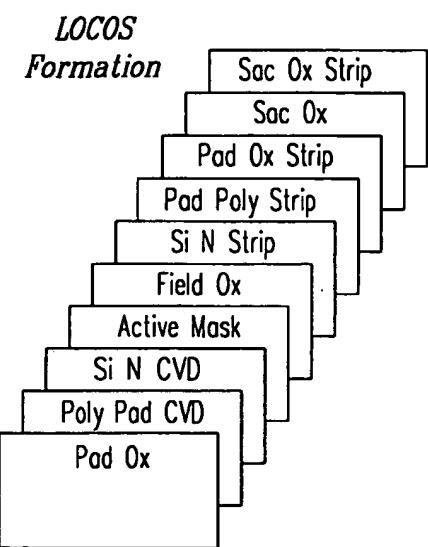


FIG. 19G

FIG. 19H



Key To
FIG. 20



Poly Cap Formation

FIG. 20A

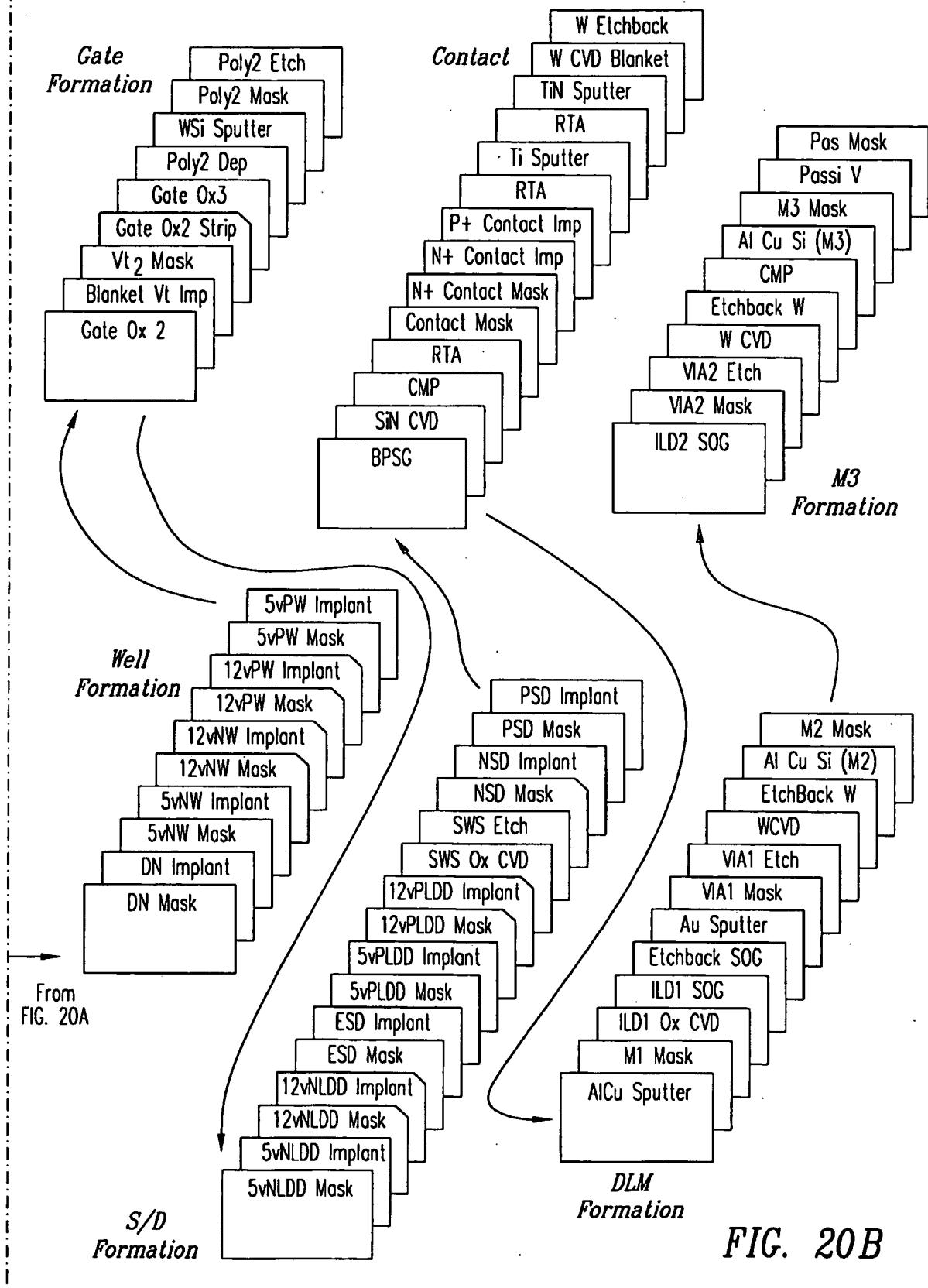
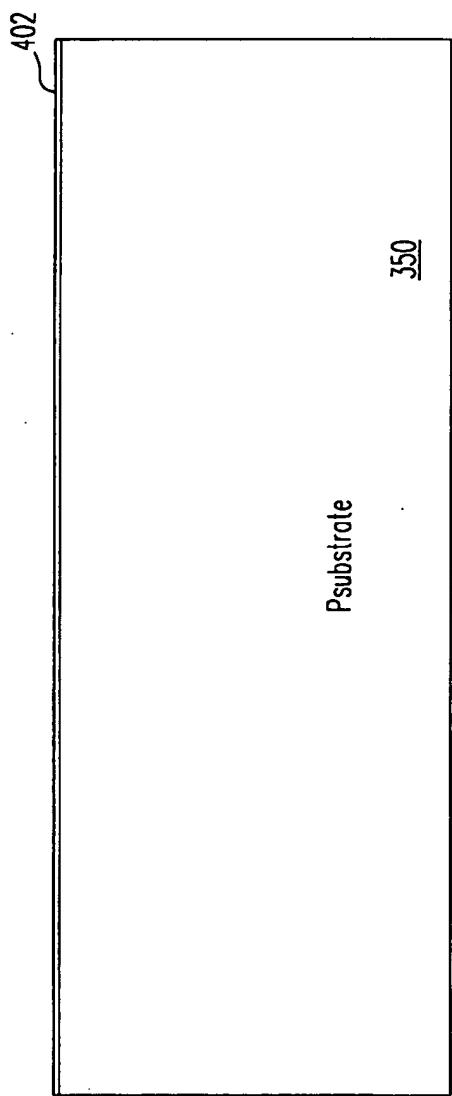


FIG. 20B

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FIG. 21



First Pad Oxide Layer

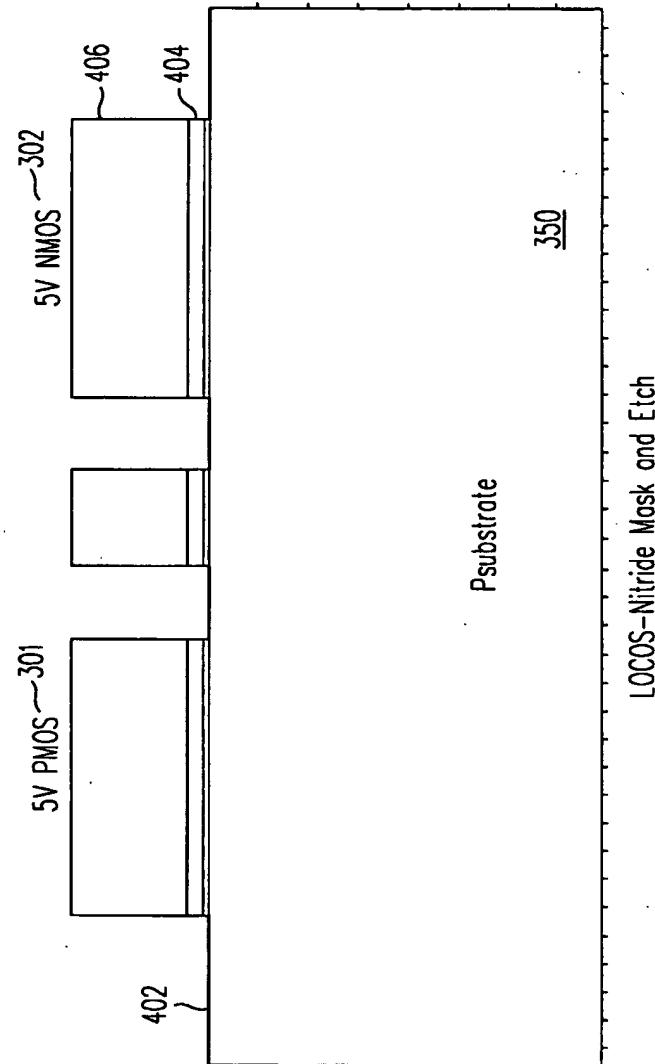


FIG. 22A

LOCOS-Nitride Mask and Etch

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FIG. 22B

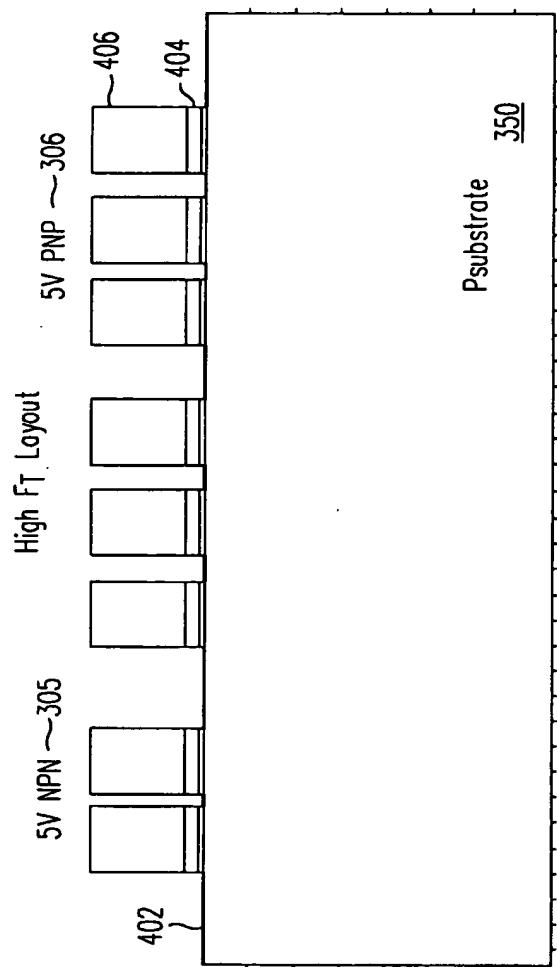
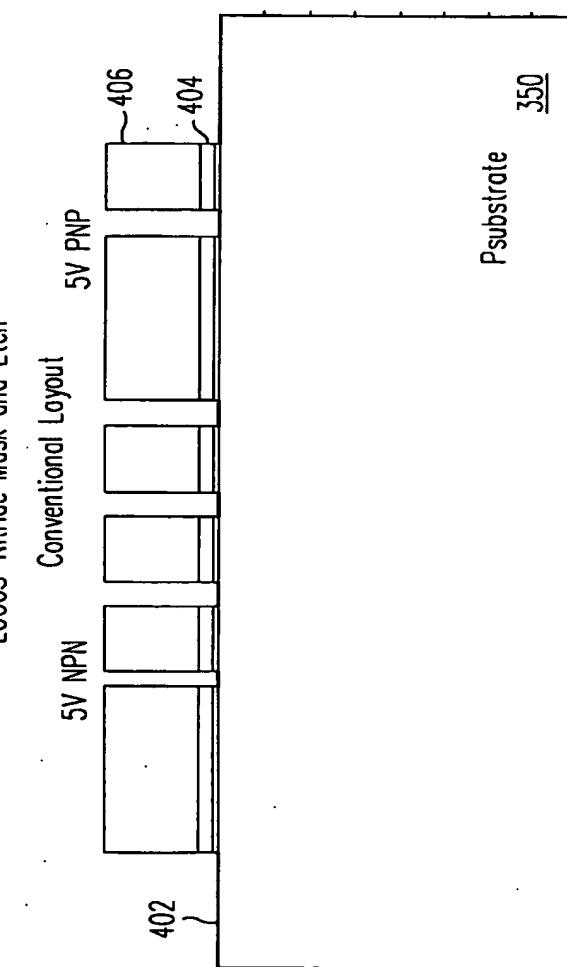


FIG. 22C



LOCOS-Nitride Mask and Etch

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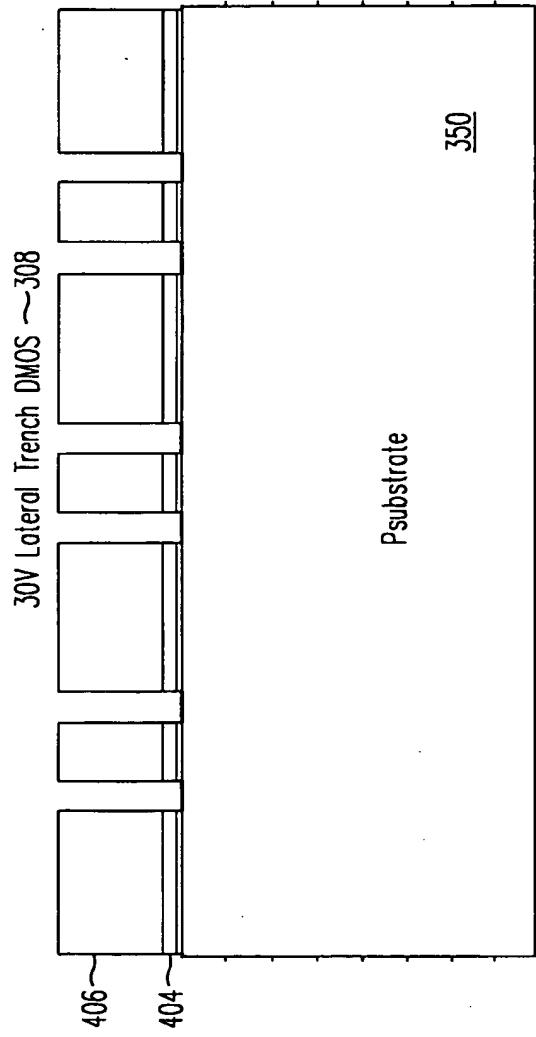
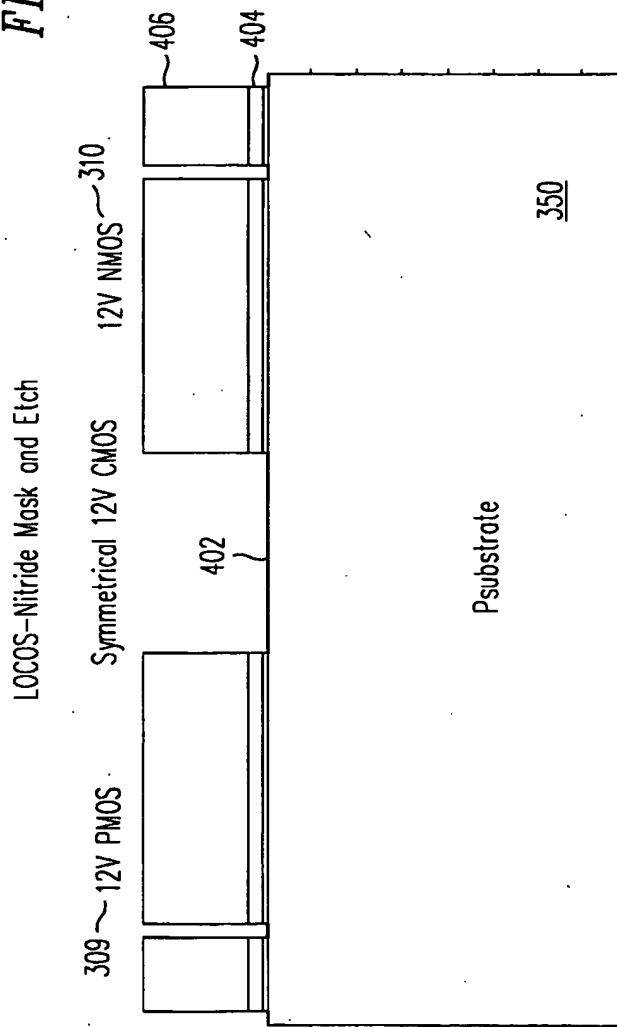


FIG. 22D

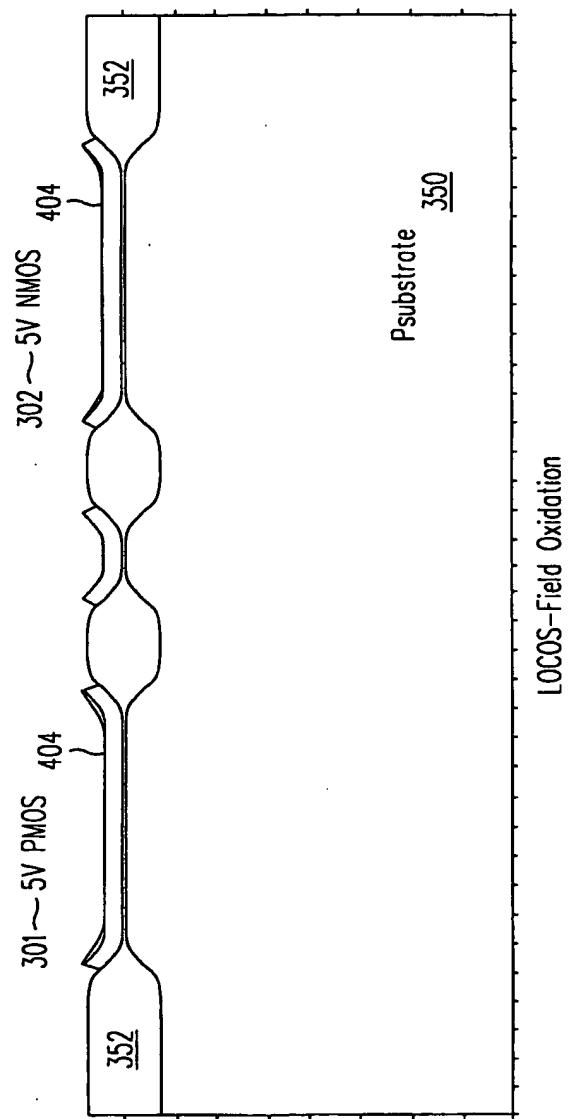


LOCOS-Nitride Mask and Etch

FIG. 22E

LOCOS-Nitride Mask and Etch

FIG. 23A



LOCOS-Field Oxidation

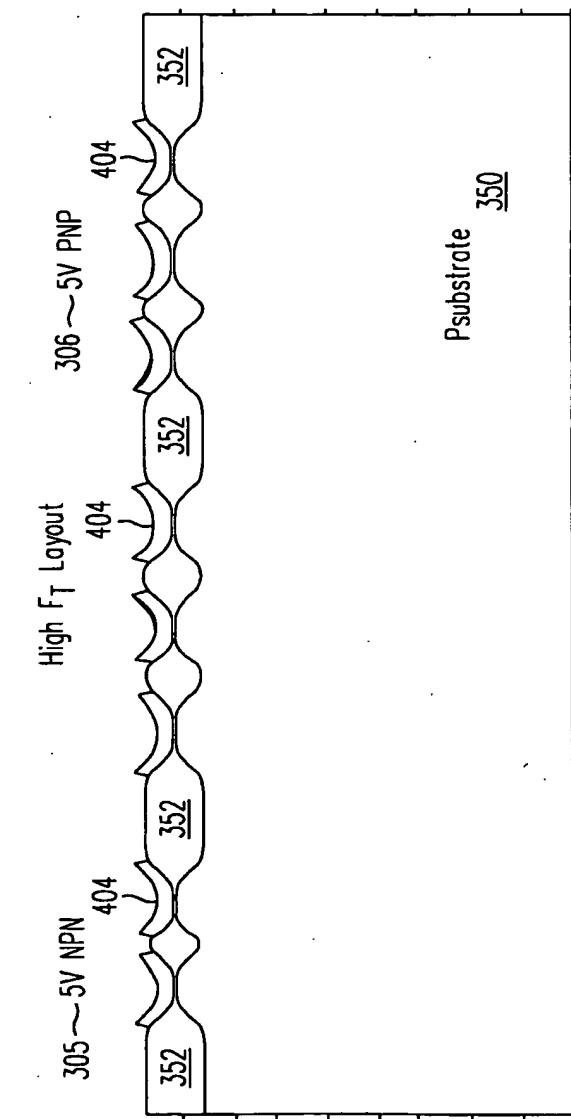


FIG. 23B

LOCOS-Field Oxidation

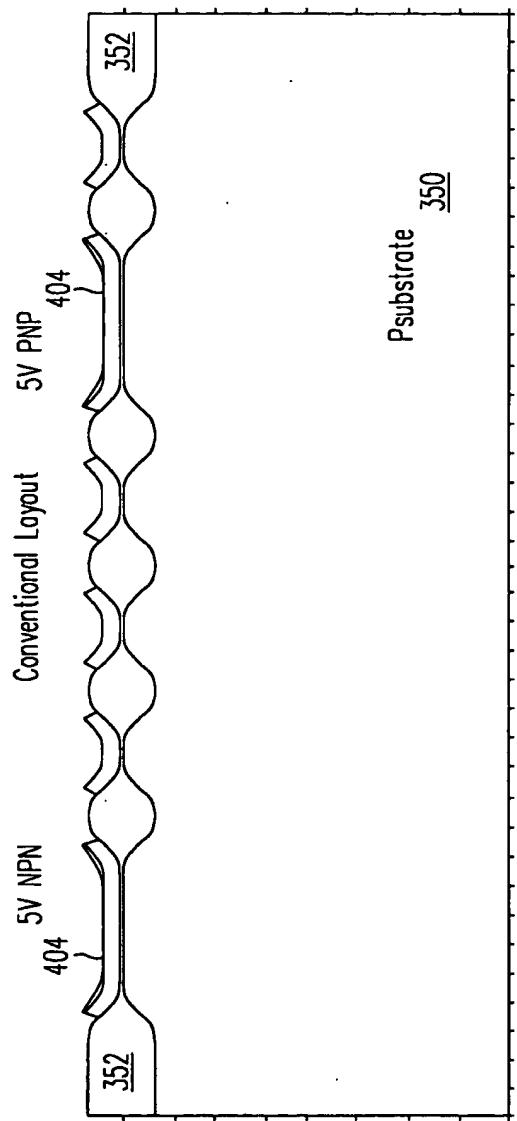


FIG. 23C

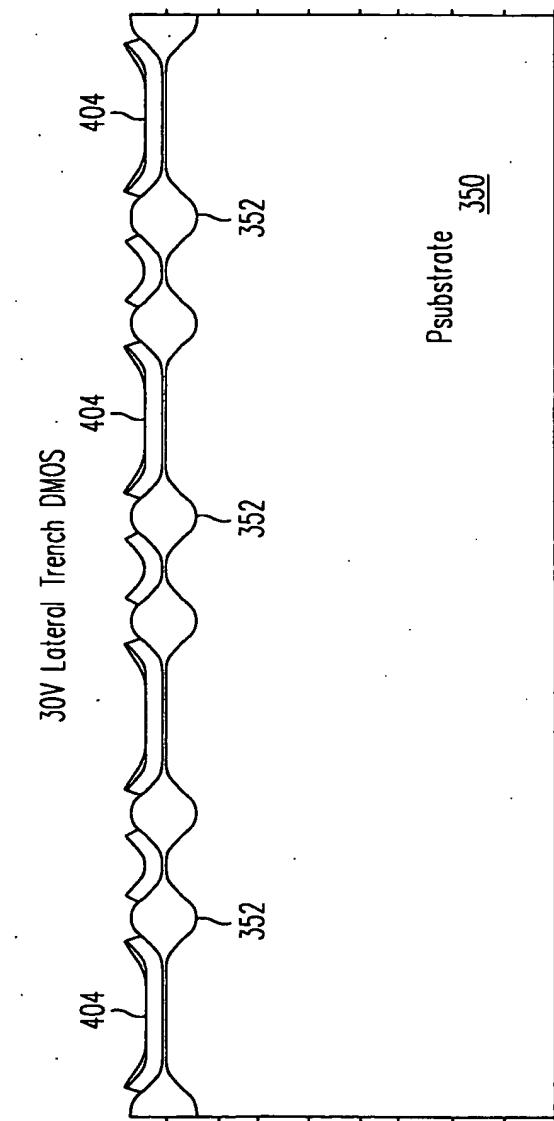


FIG. 23D

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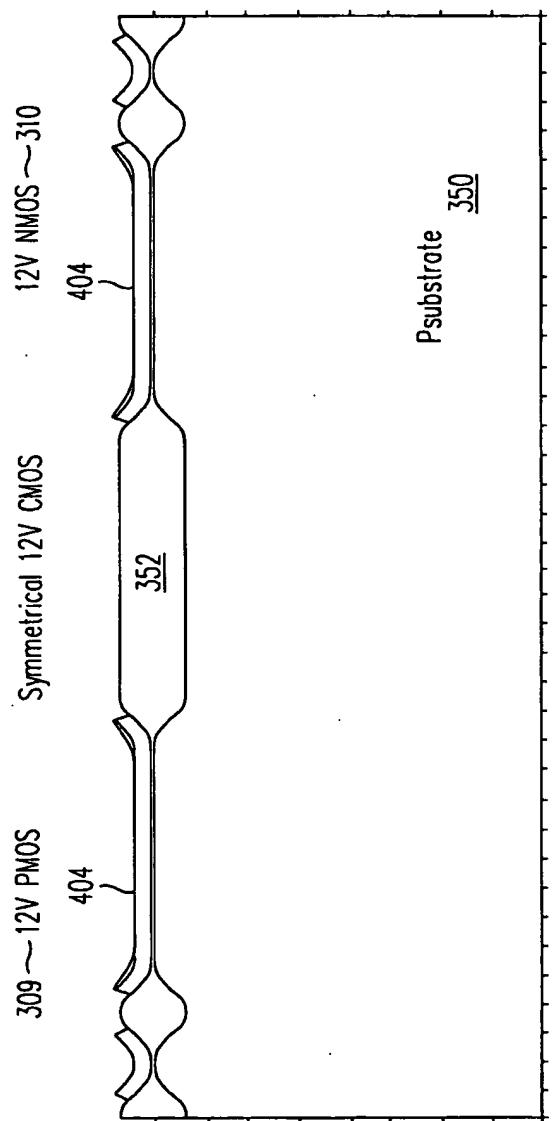


FIG. 23E

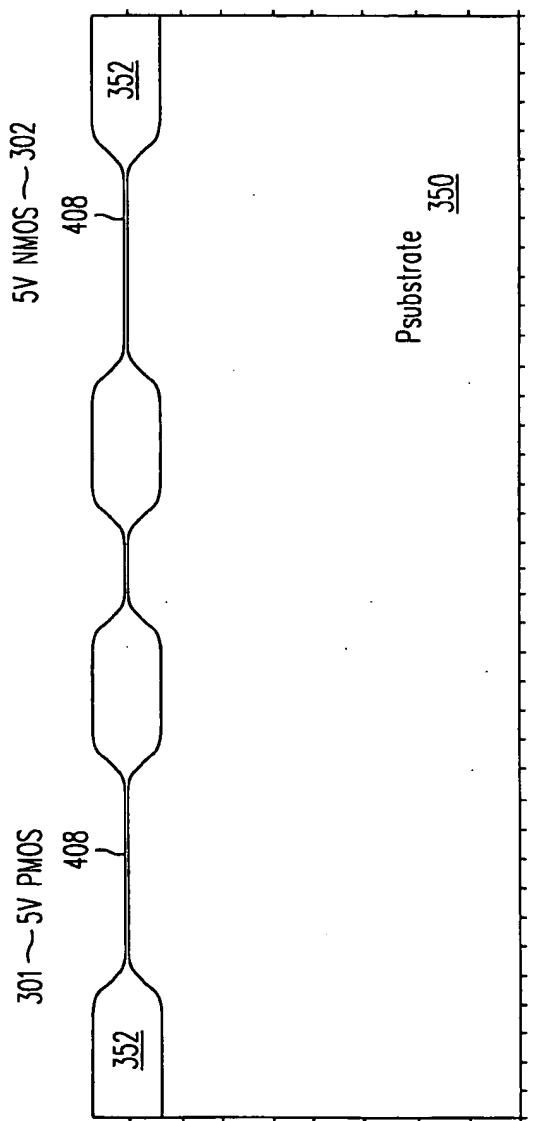


FIG. 24A

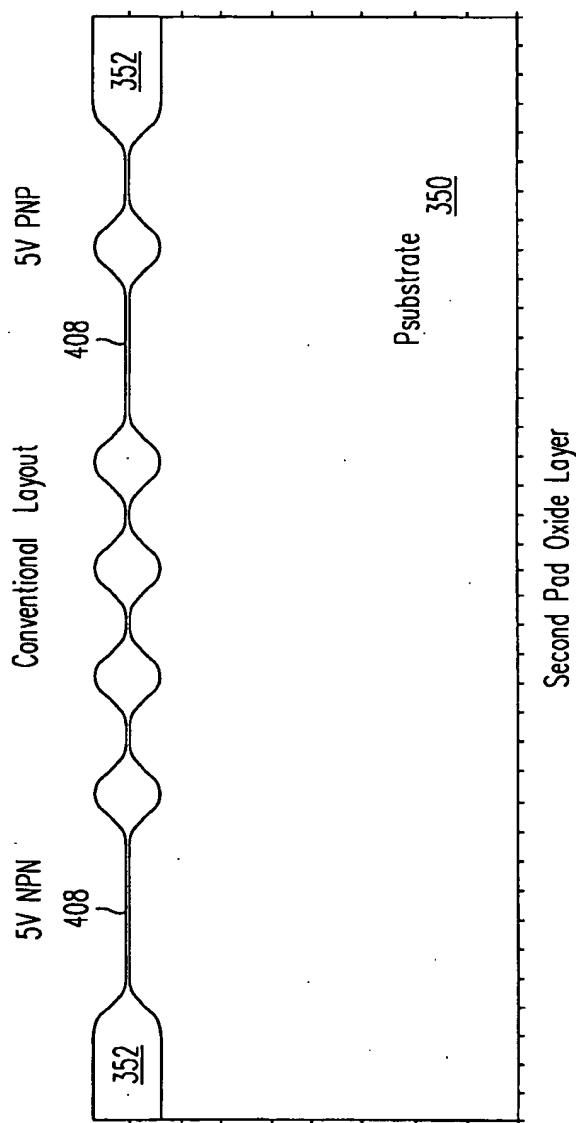
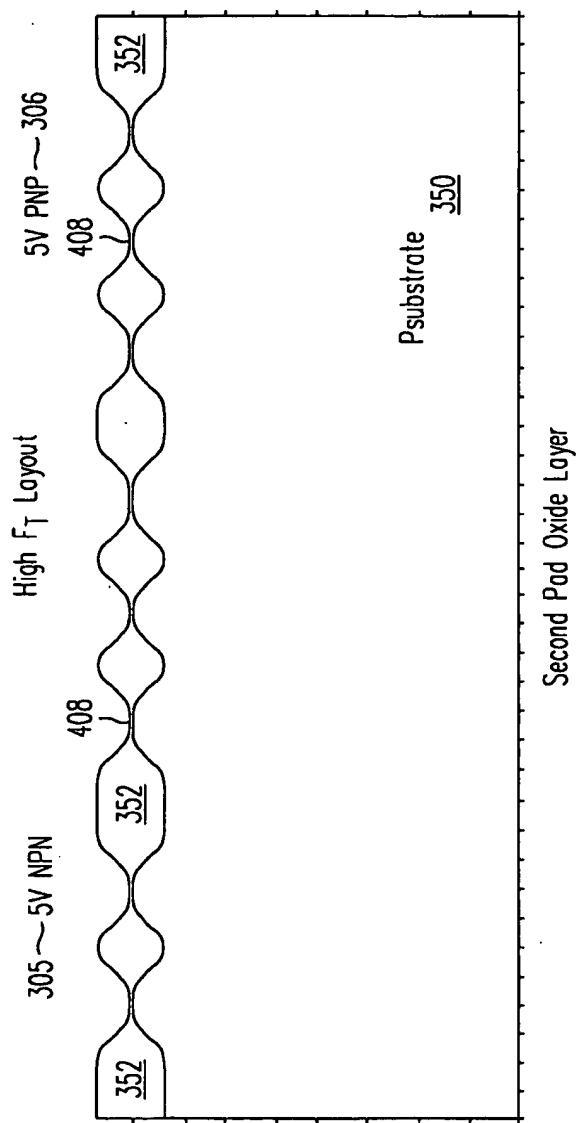
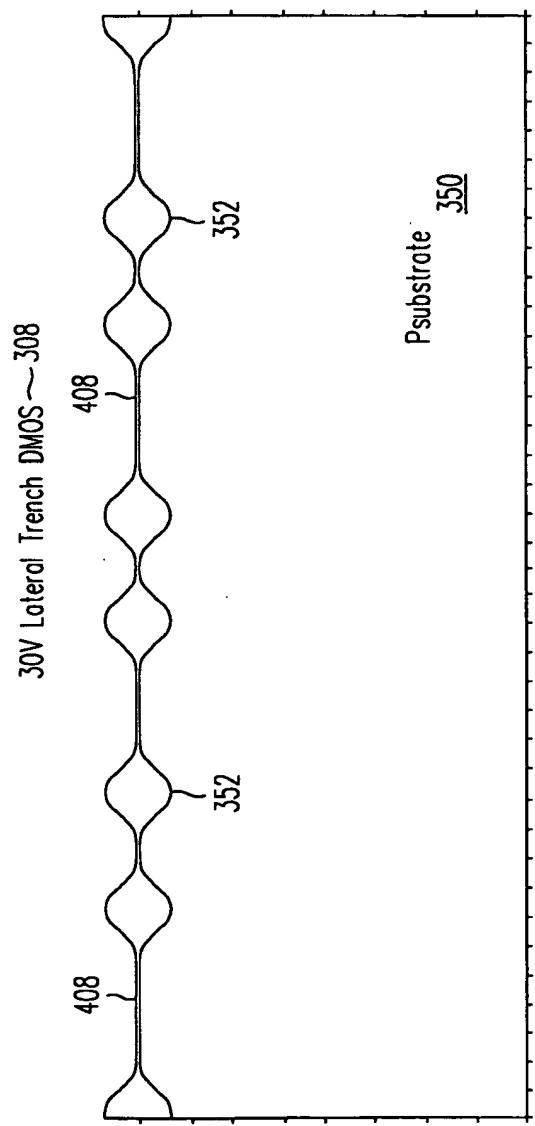
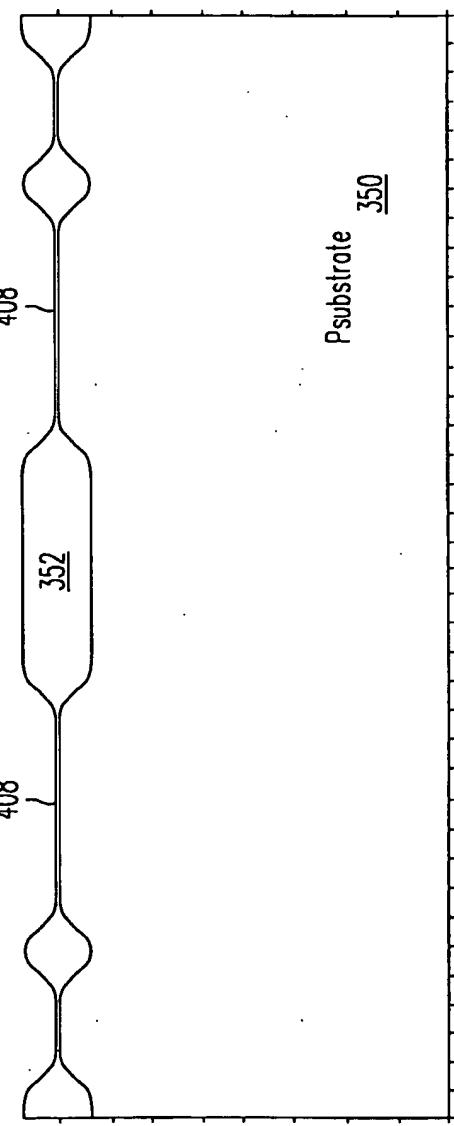


FIG. 24D



30V Lateral Trench DMOS ~ 308
309 ~ 12V PMOS
Symmetrical 12V CMOS
12V NMOS ~ 310

FIG. 24E



Second Pad Oxide Layer

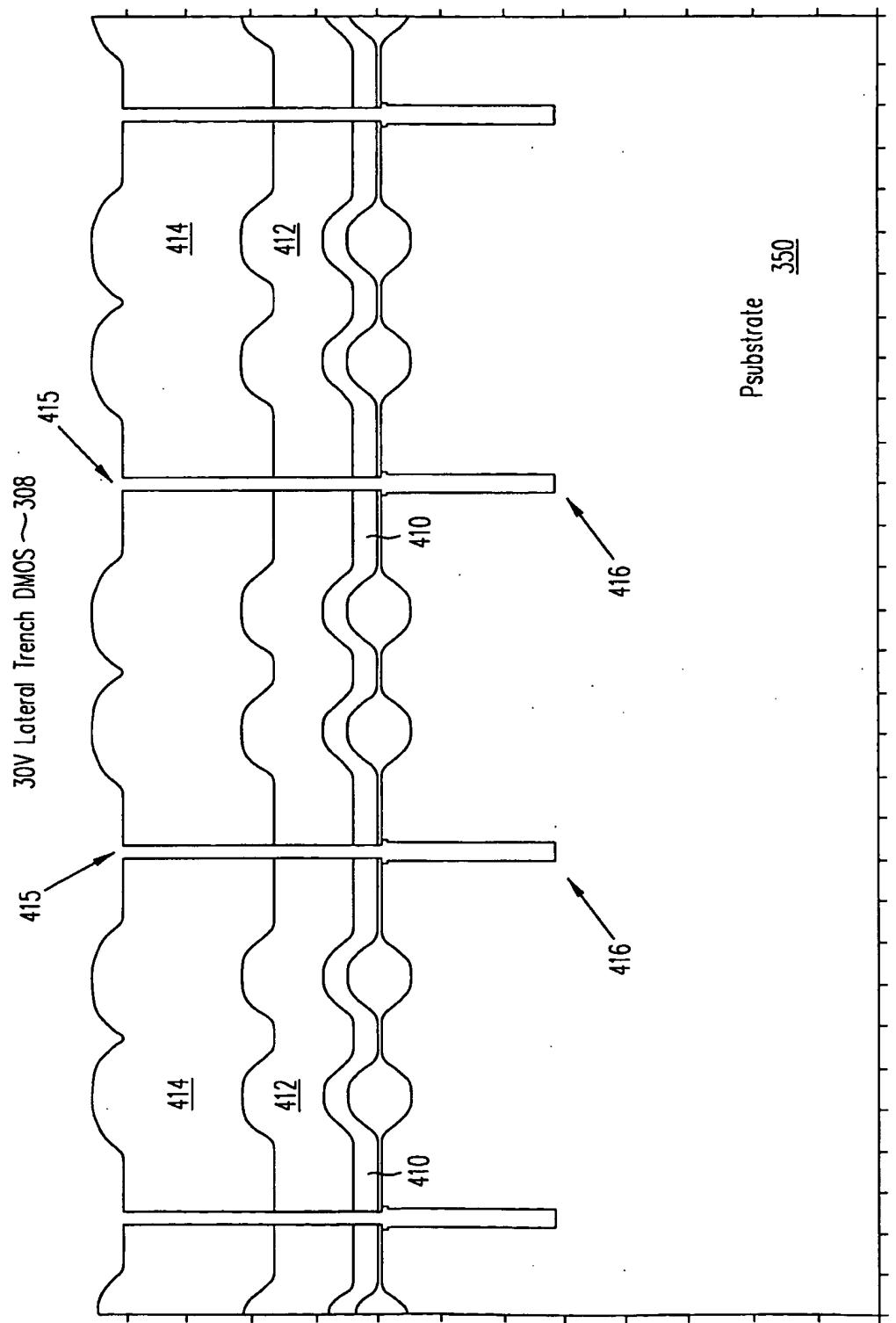


FIG. 25D

Trench Hard Mask

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30V Lateral Trench DMOS ~308

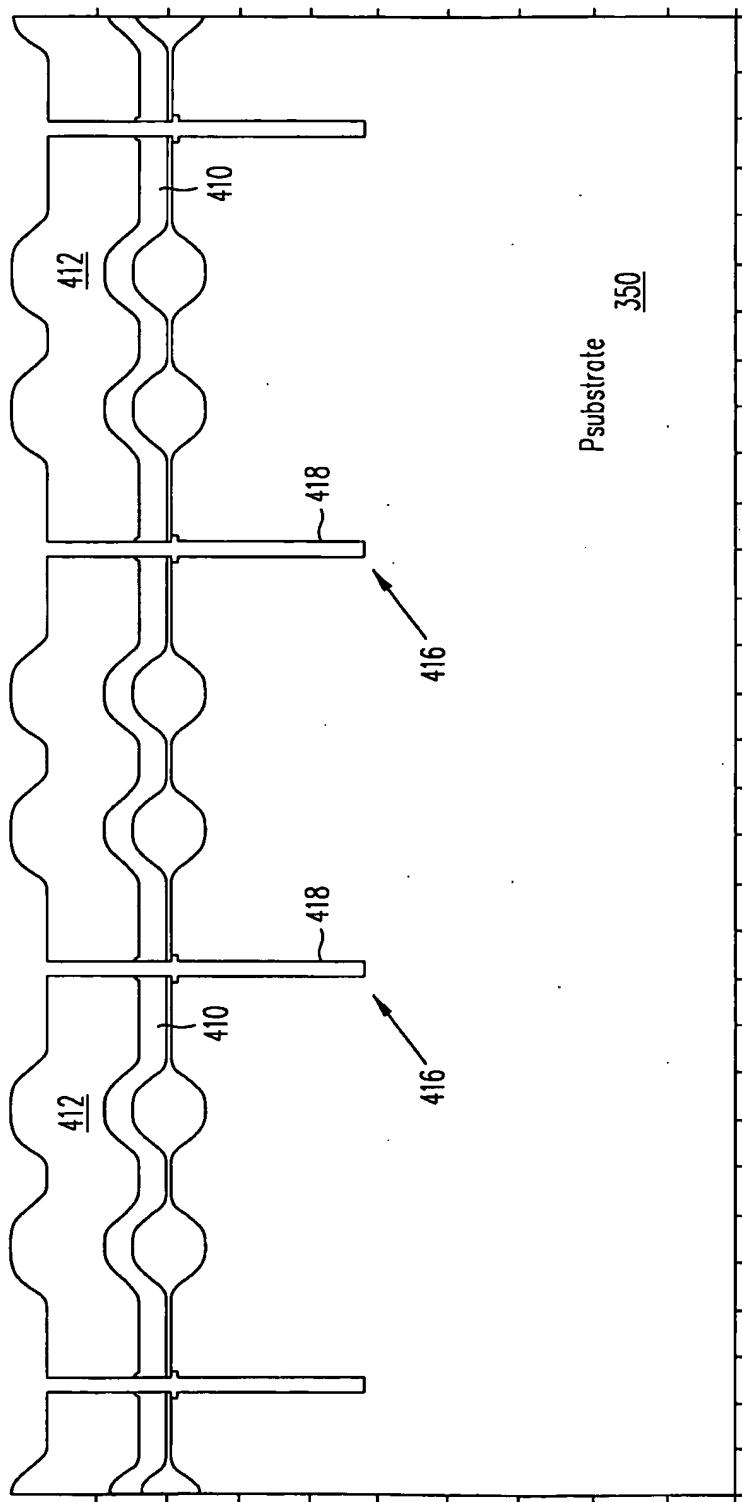


FIG. 26D

30V Lateral Trench DMOS ~308

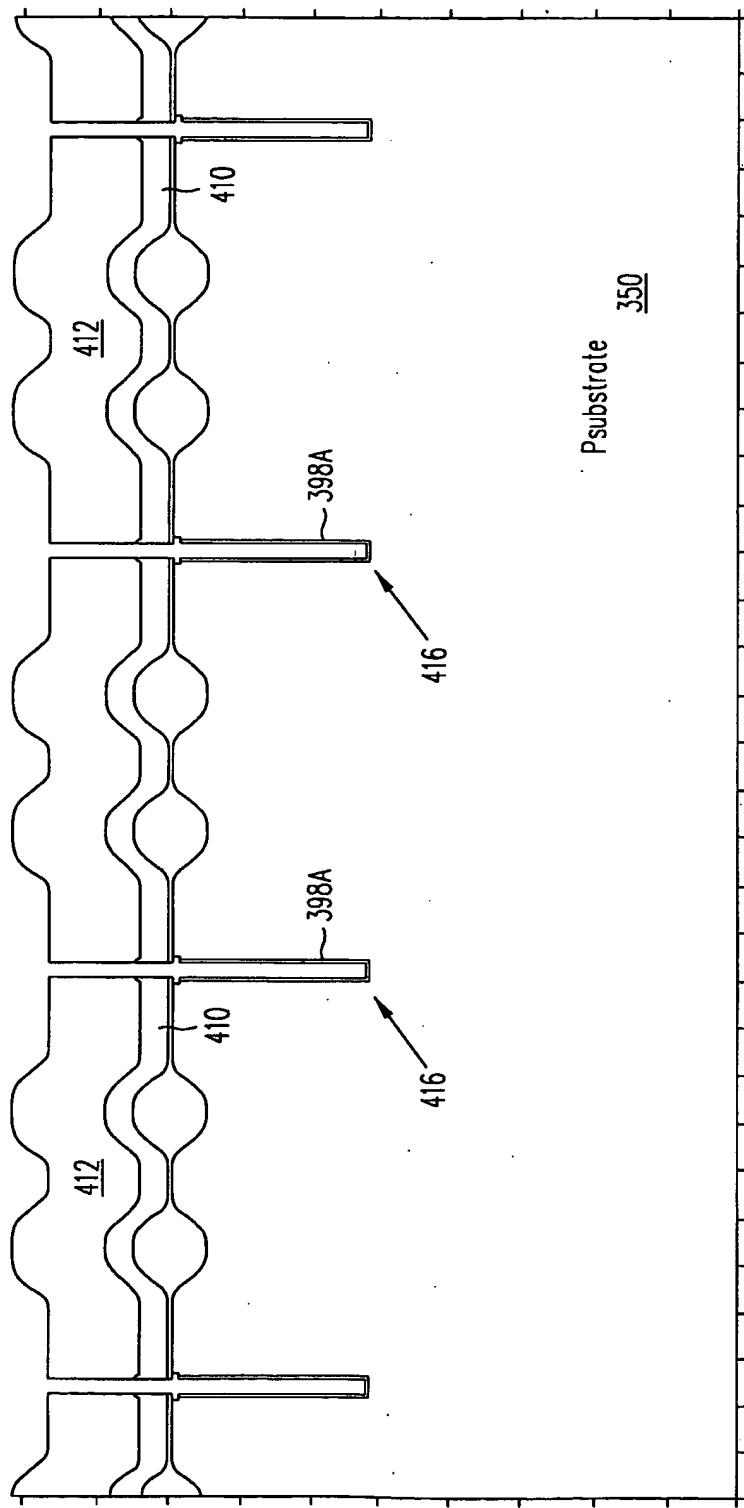
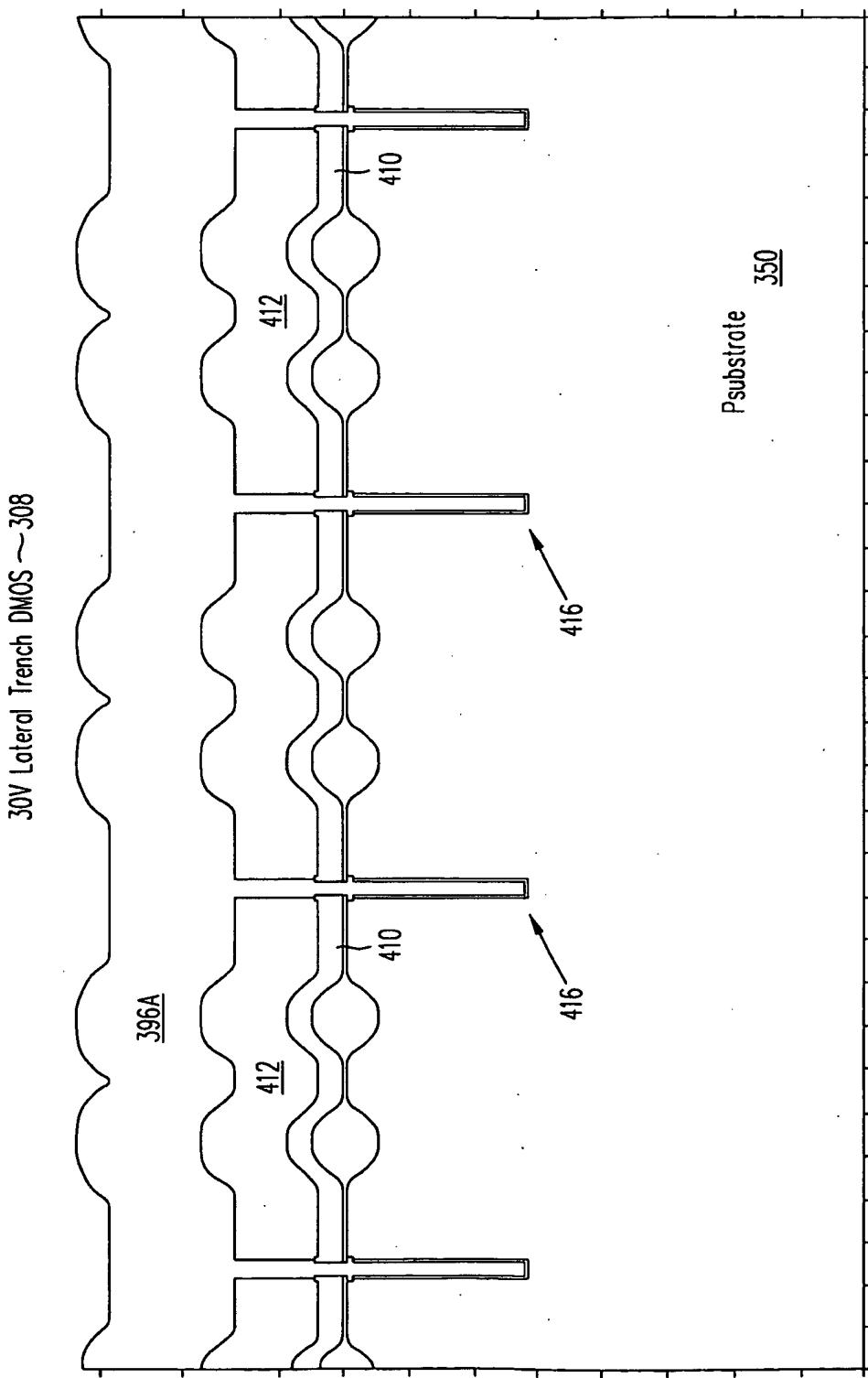


FIG. 27D

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Polysilicon-First Layer

FIG. 28D

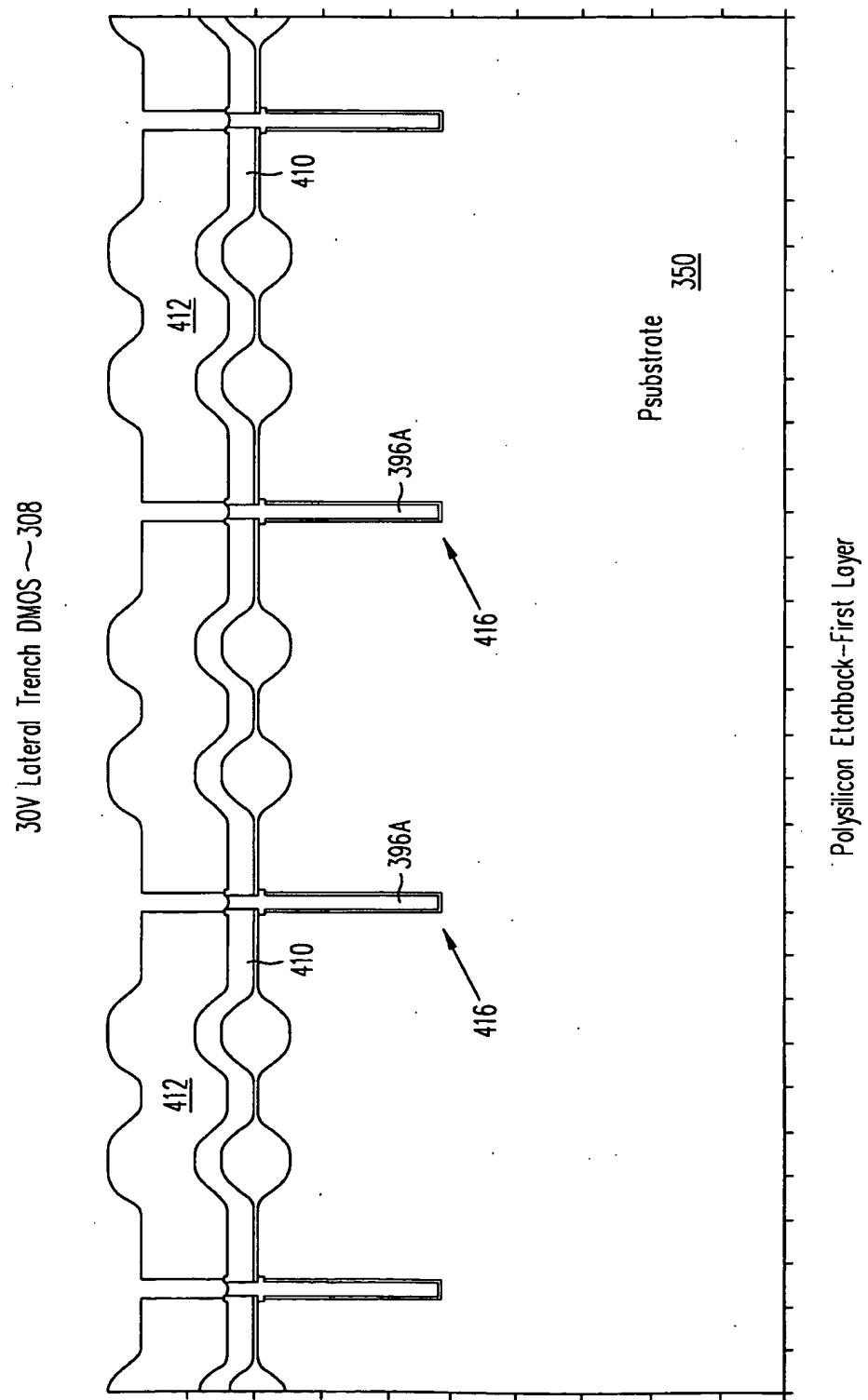


FIG. 29D

Poly-silicon Etchback-First Layer

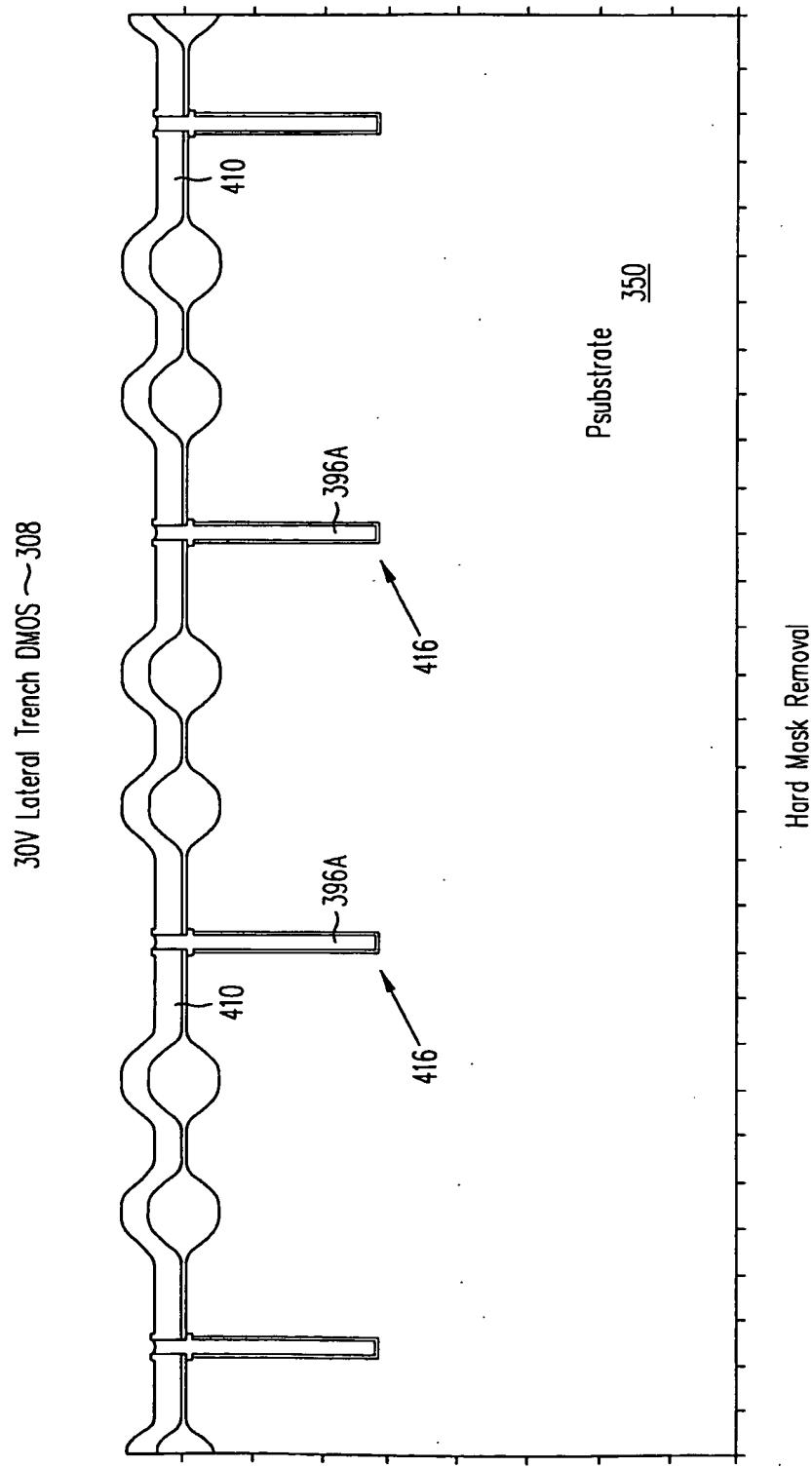


FIG. 30D

Hard Mask Removal

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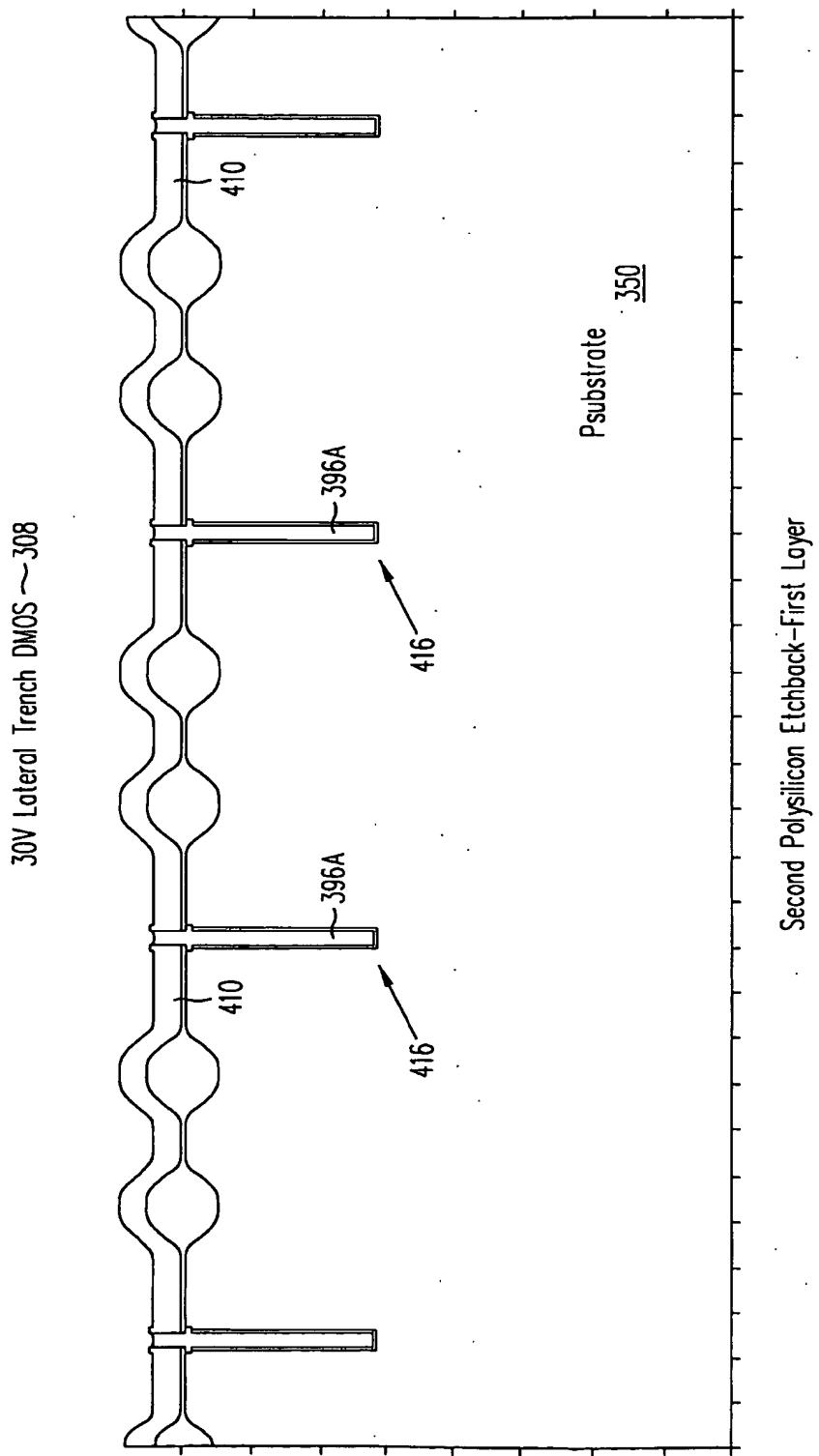


FIG. 31D

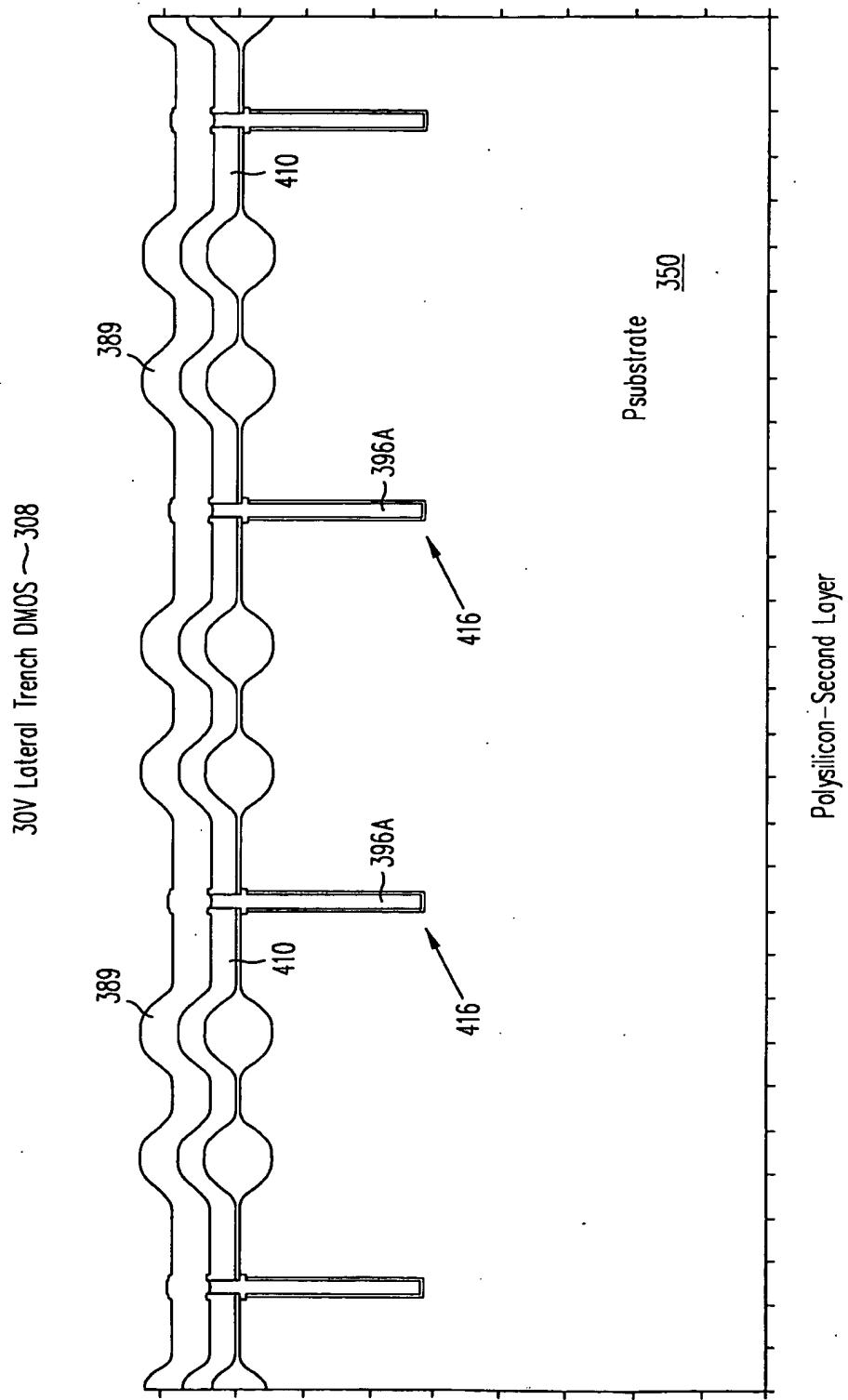


FIG. 32D

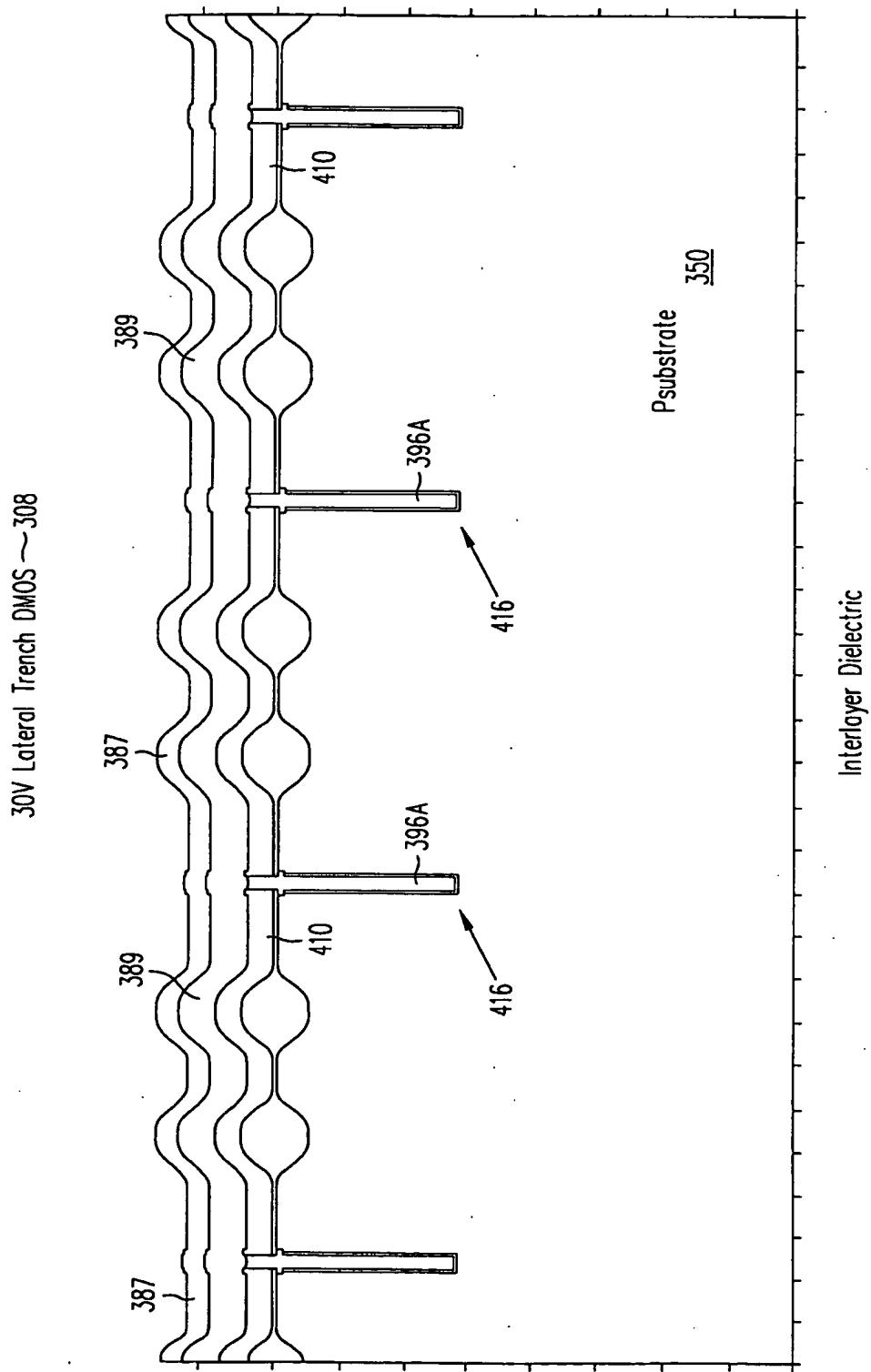
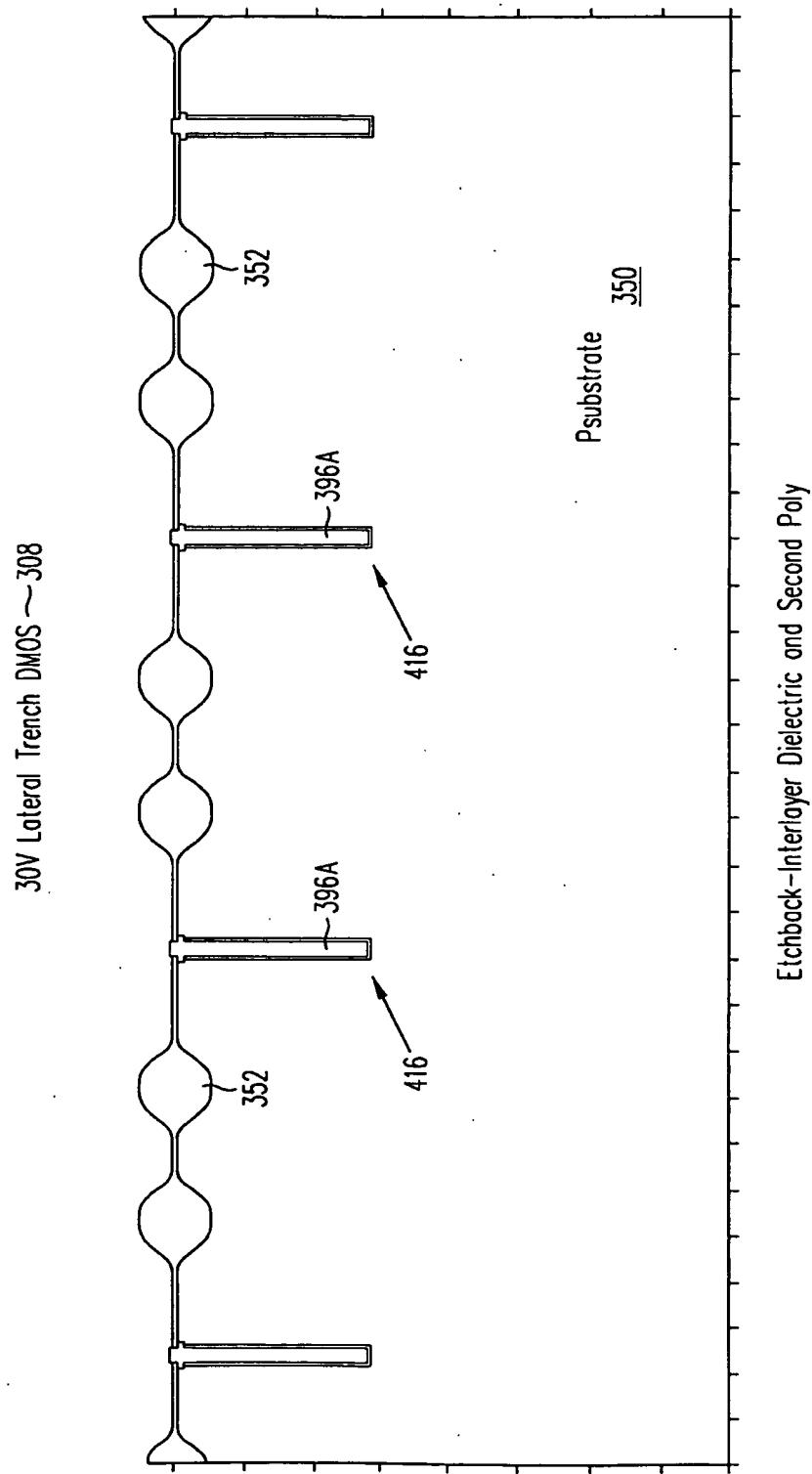
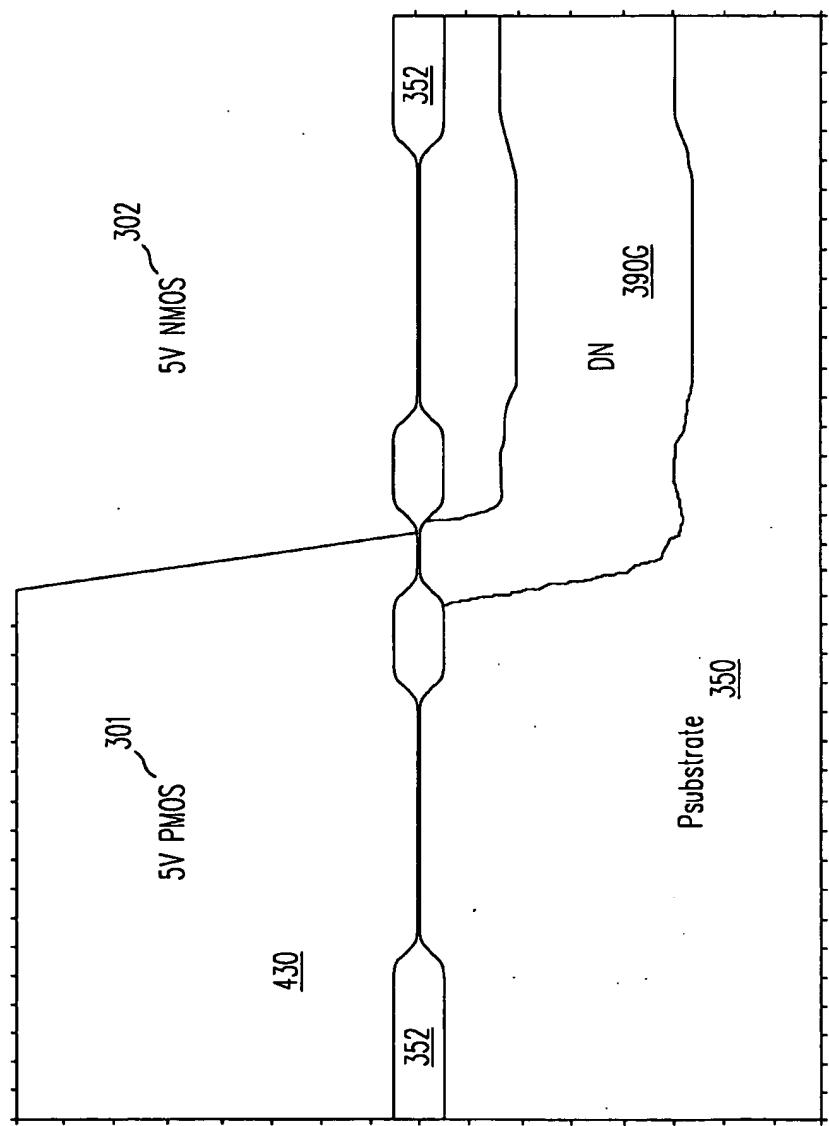


FIG. 33D



Etchback-Interlayer Dielectric and Second Poly

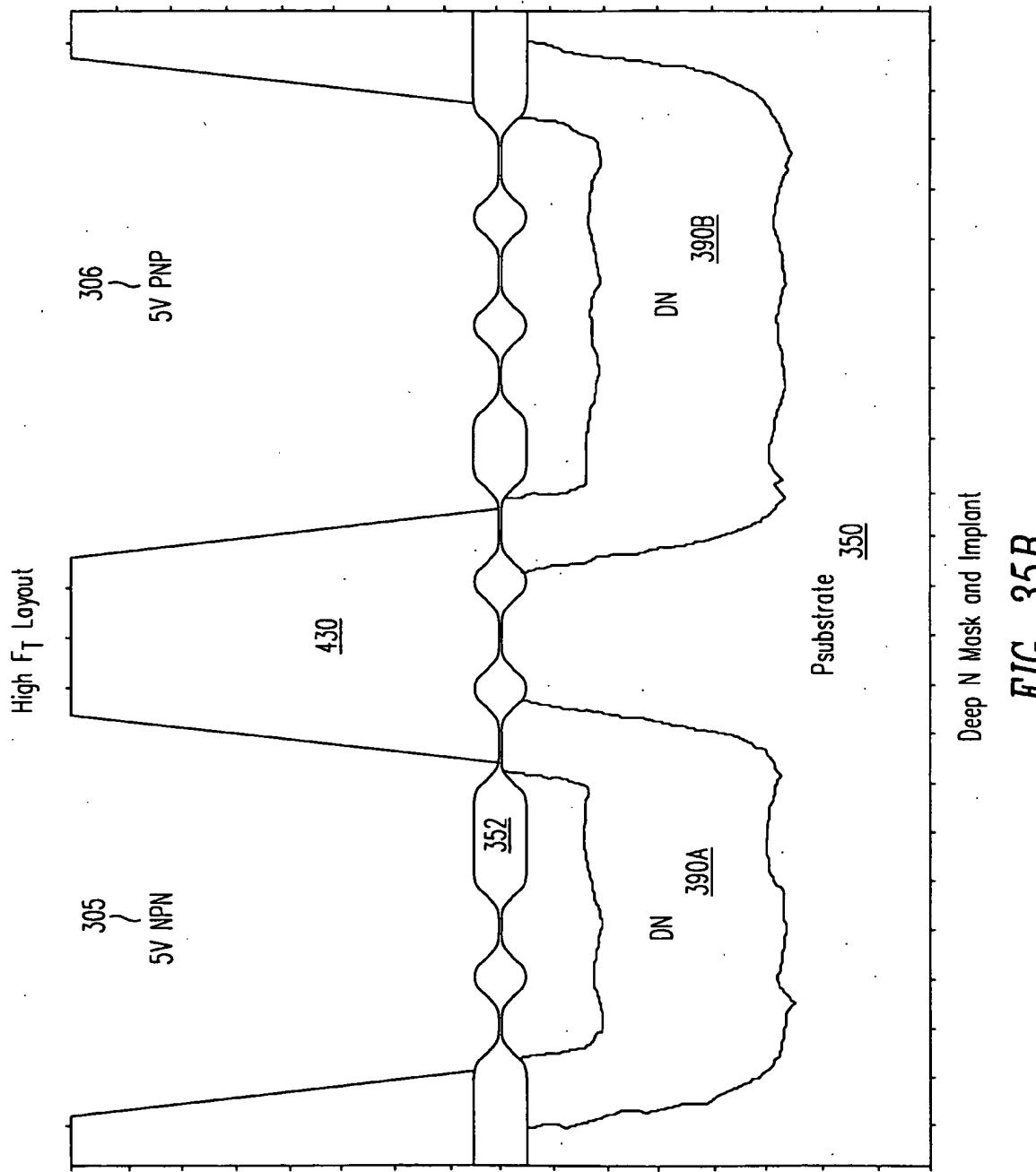
FIG. 34D



Deep N Mask and implant

FIG. 35A

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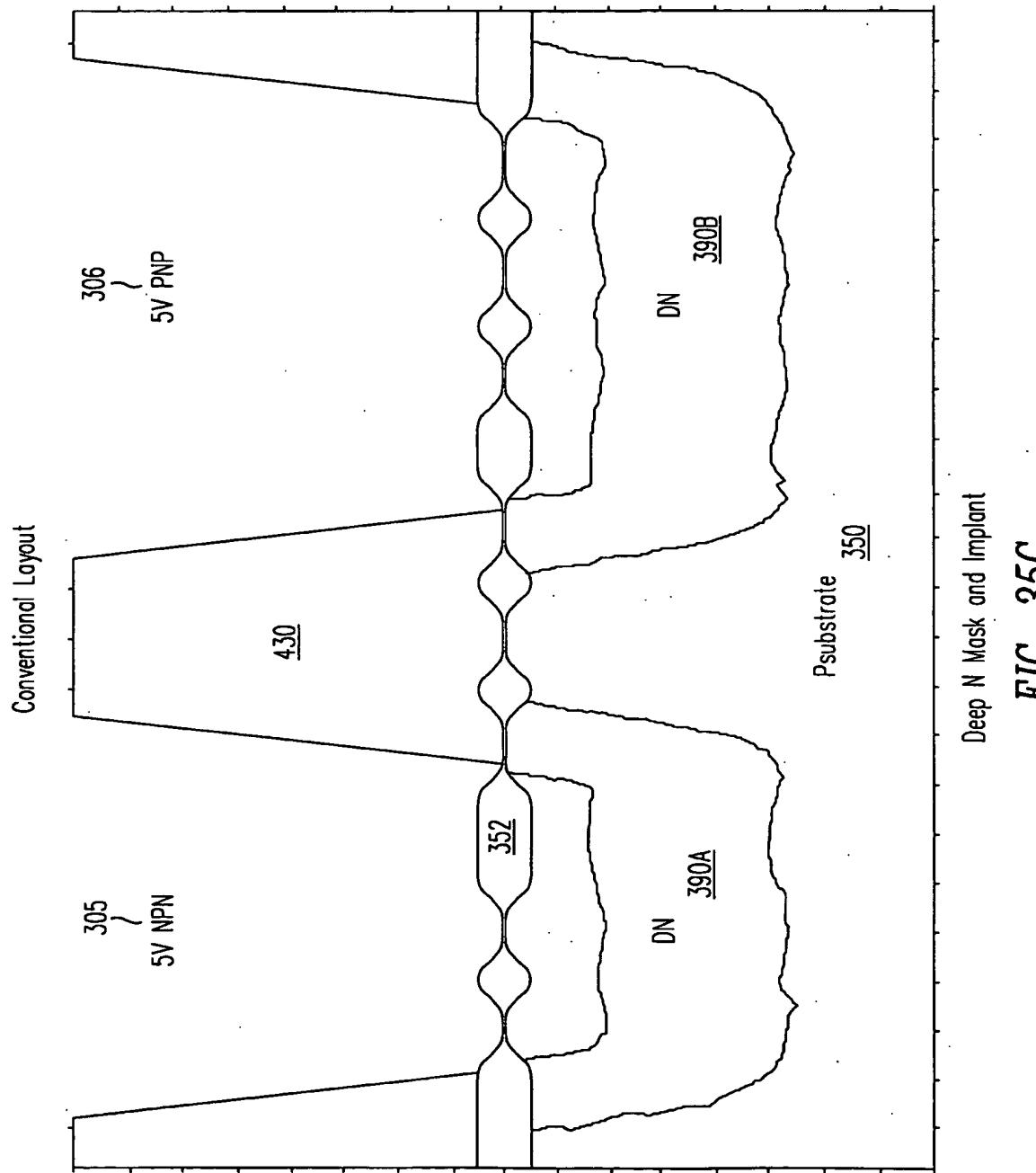


FIG. 35C

Deep N Mask and Implant

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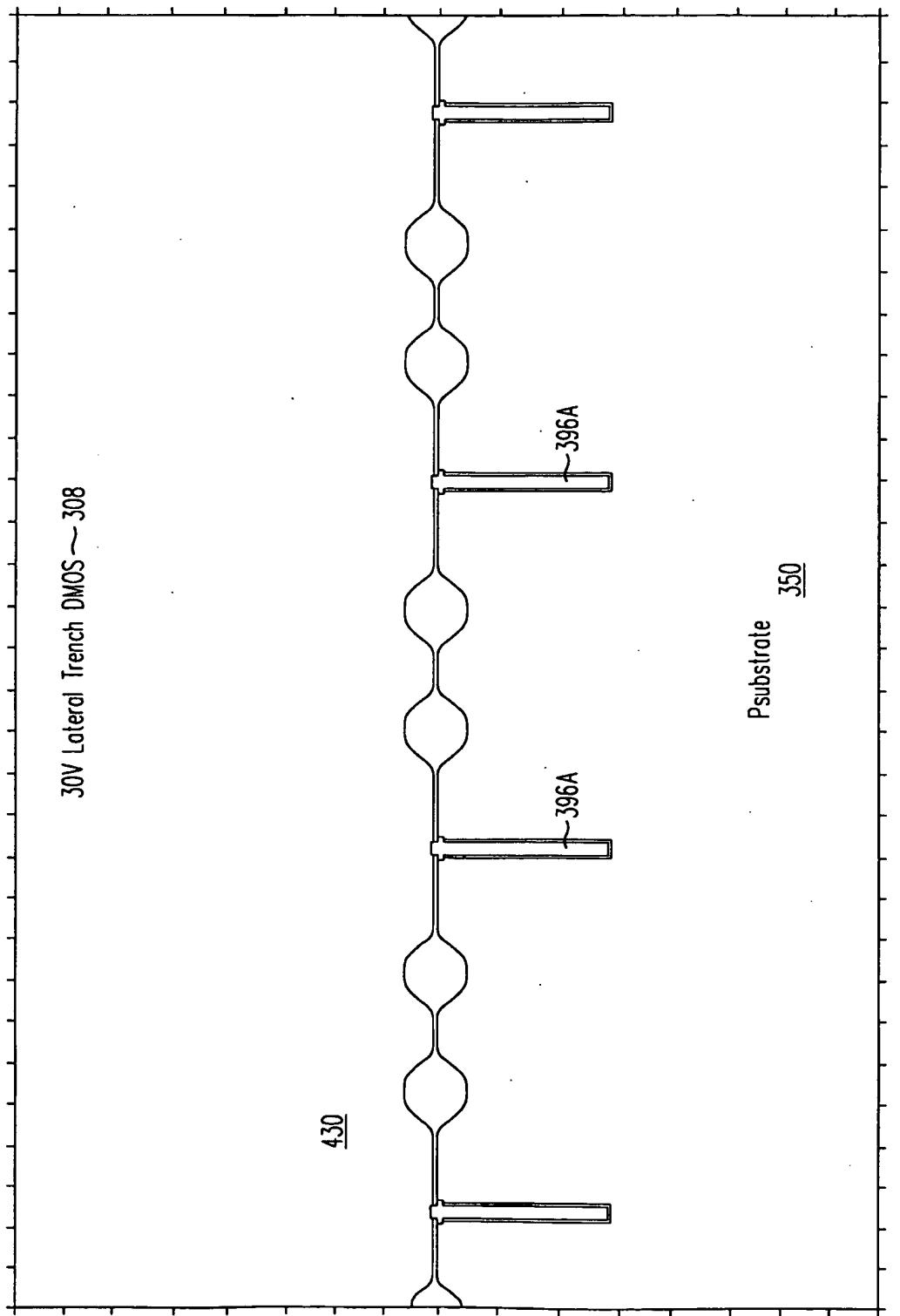
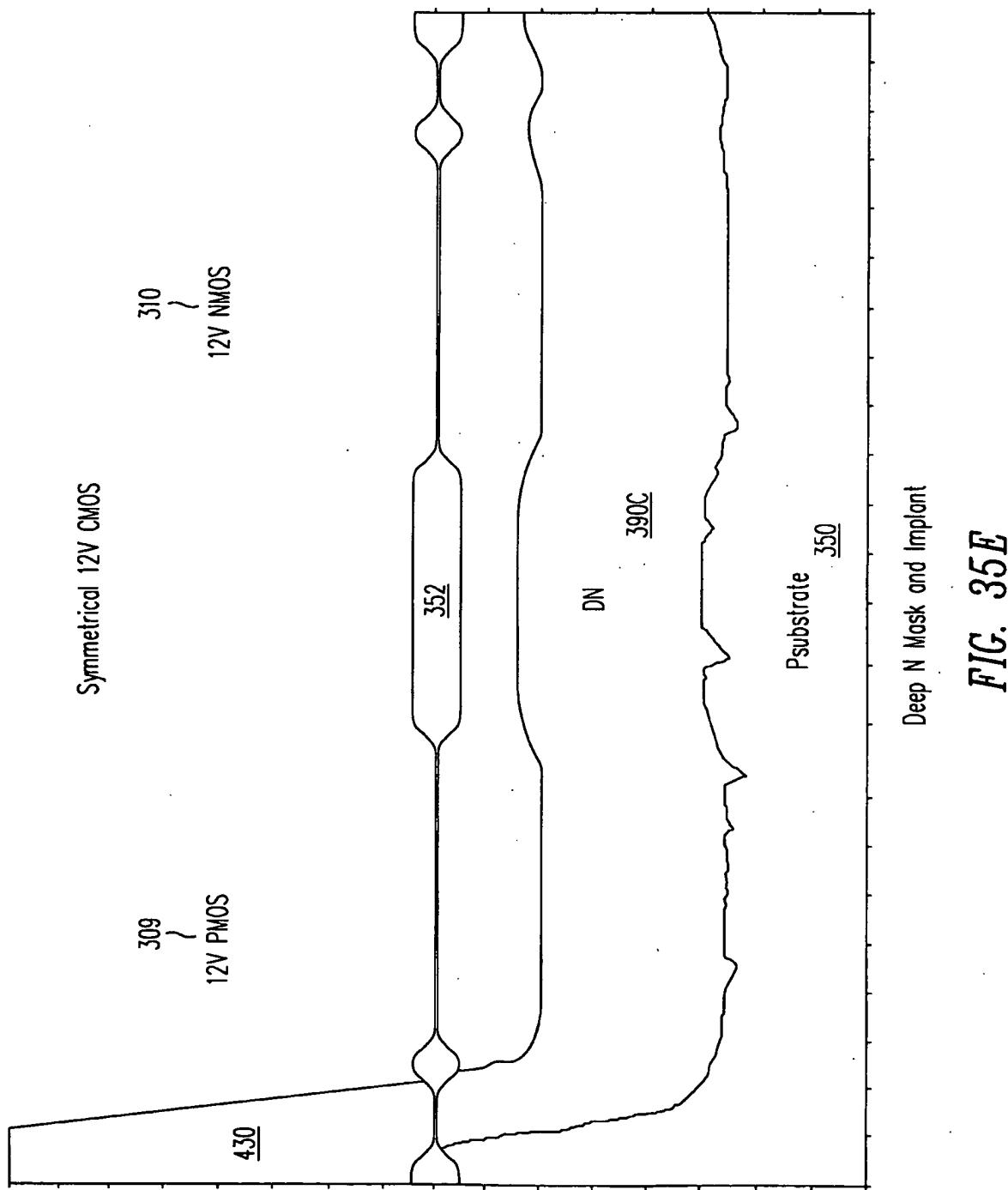


FIG. 35D

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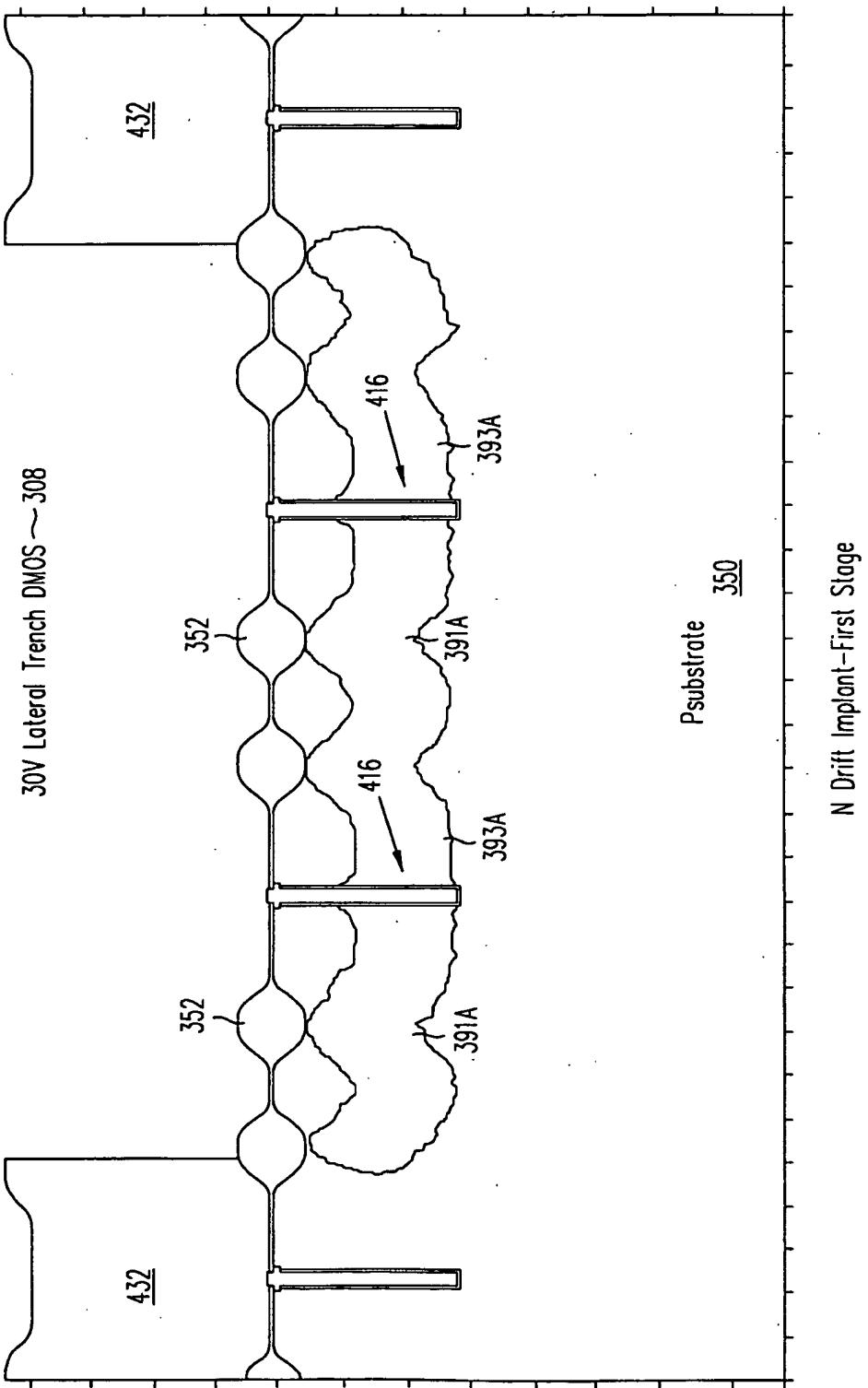


FIG. 36D

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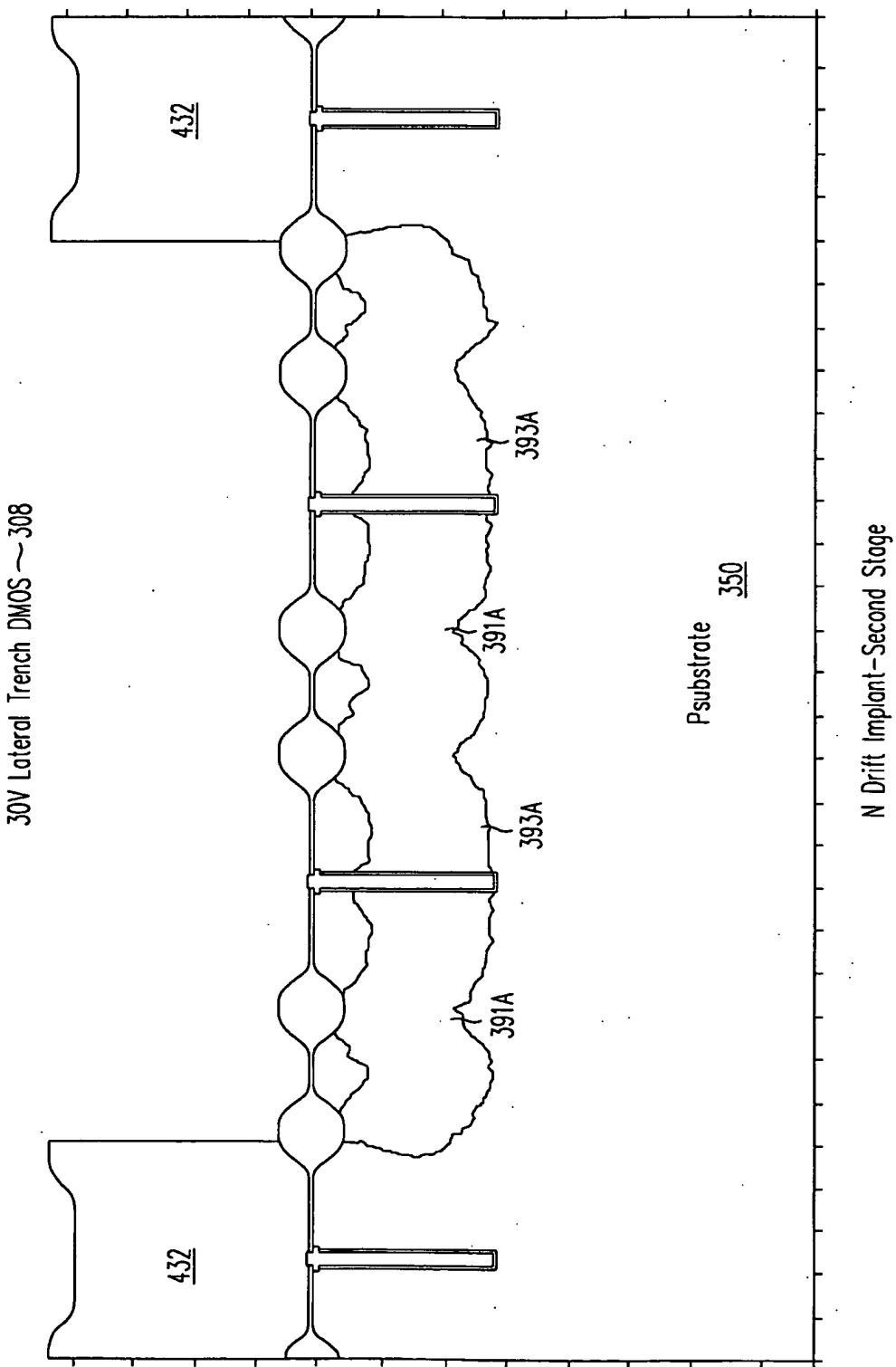
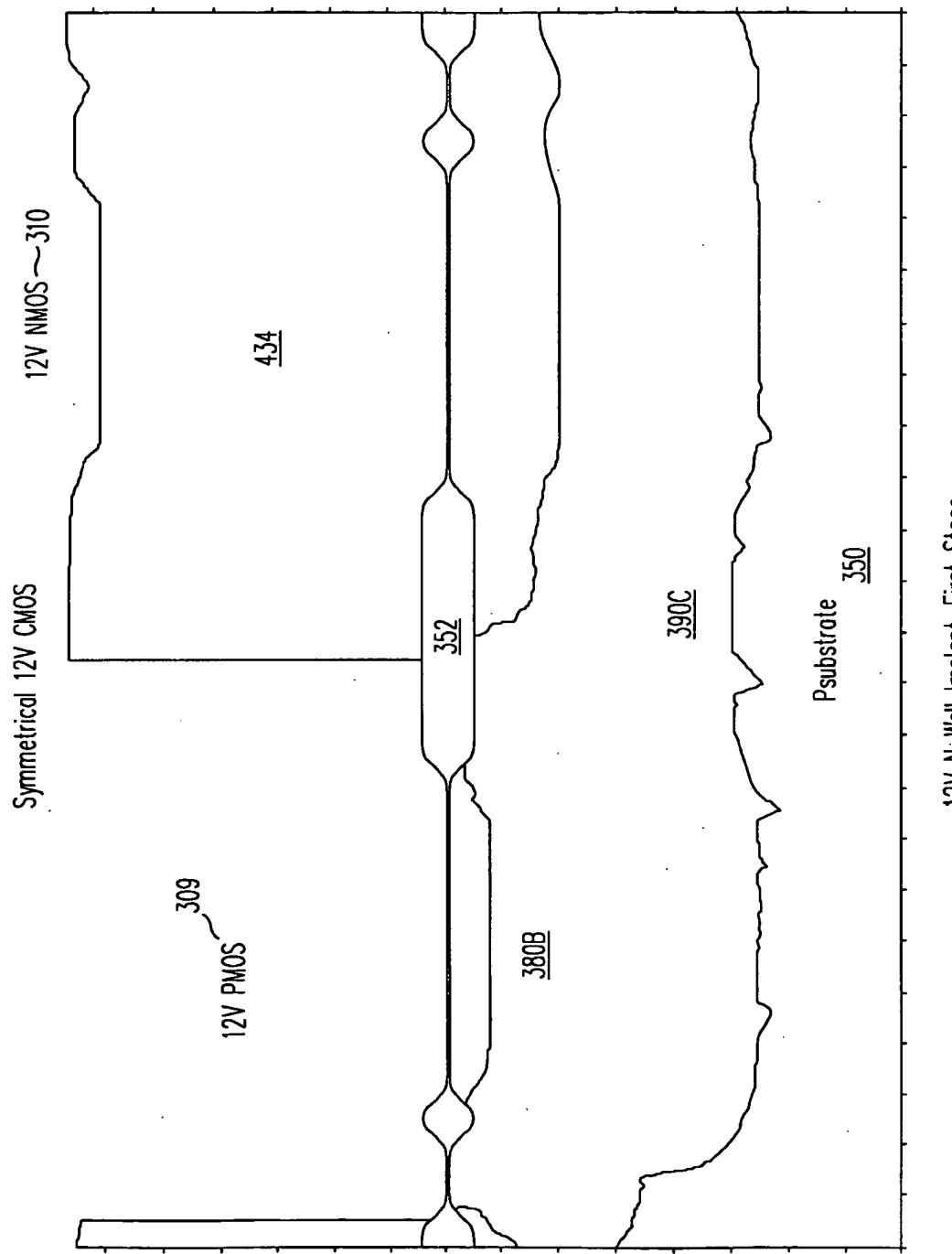
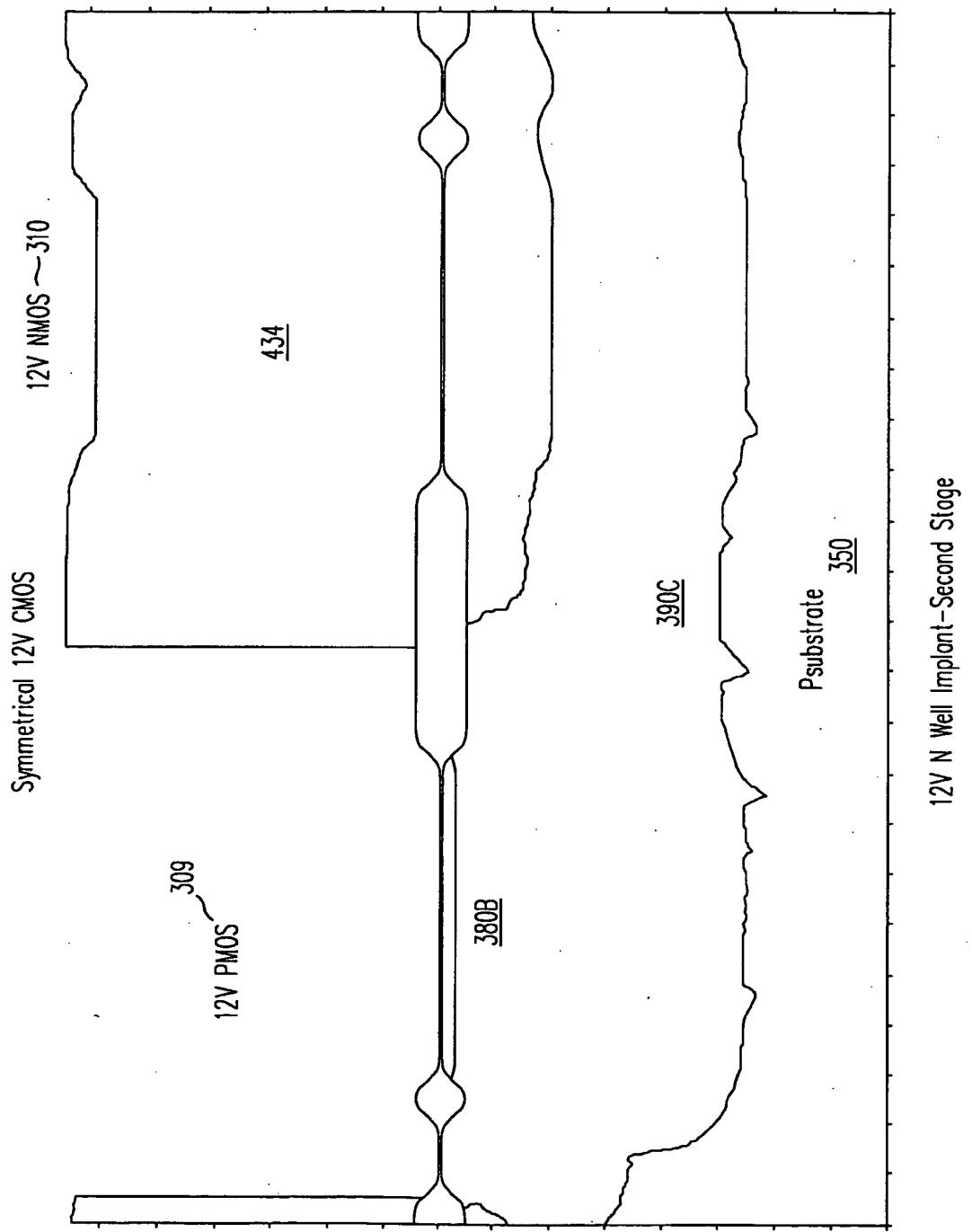


FIG. 37D

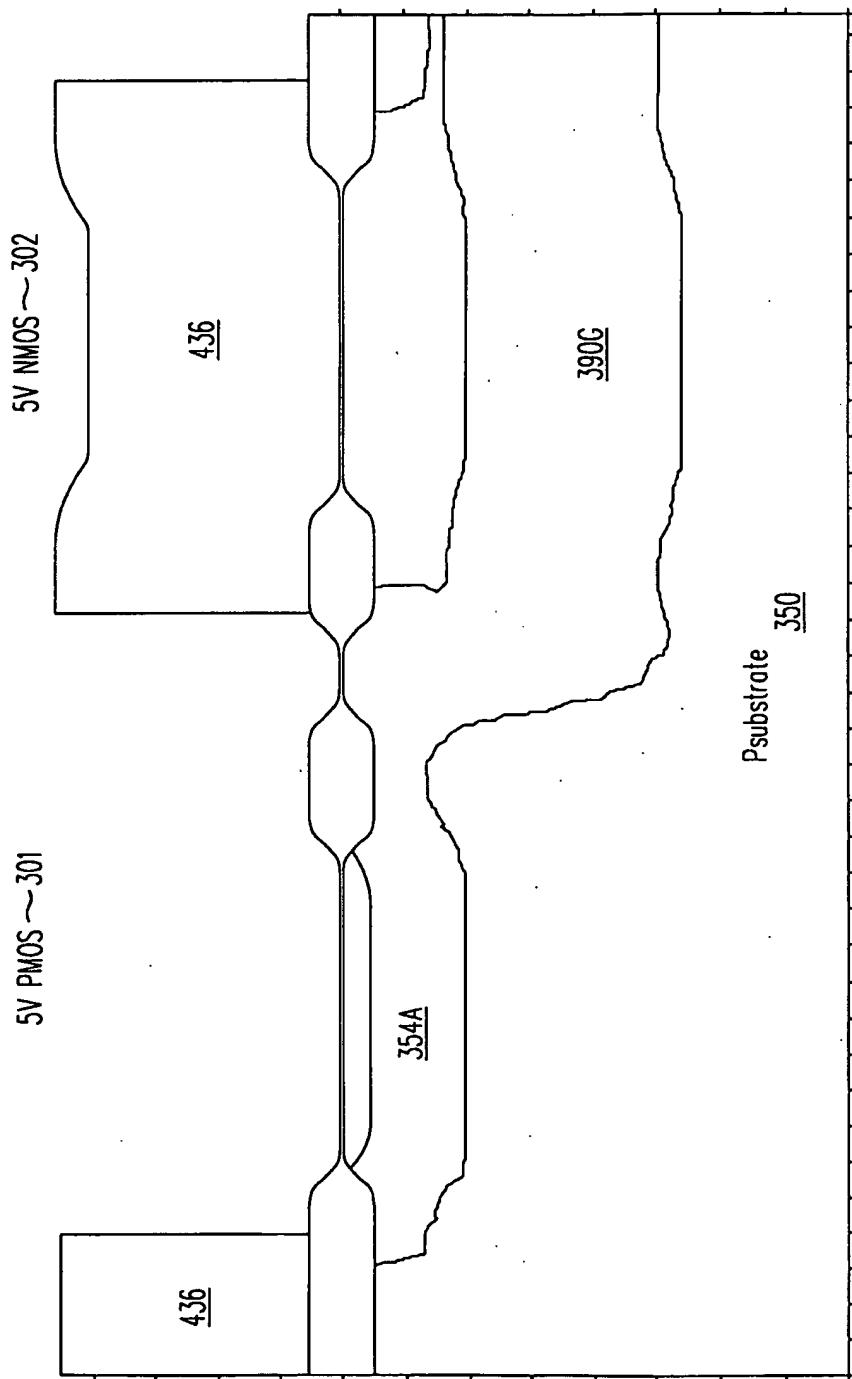


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12V N Well Implant-Second Stage

FIG. 39E



5V N Well Implant-First Stage

FIG. 40A

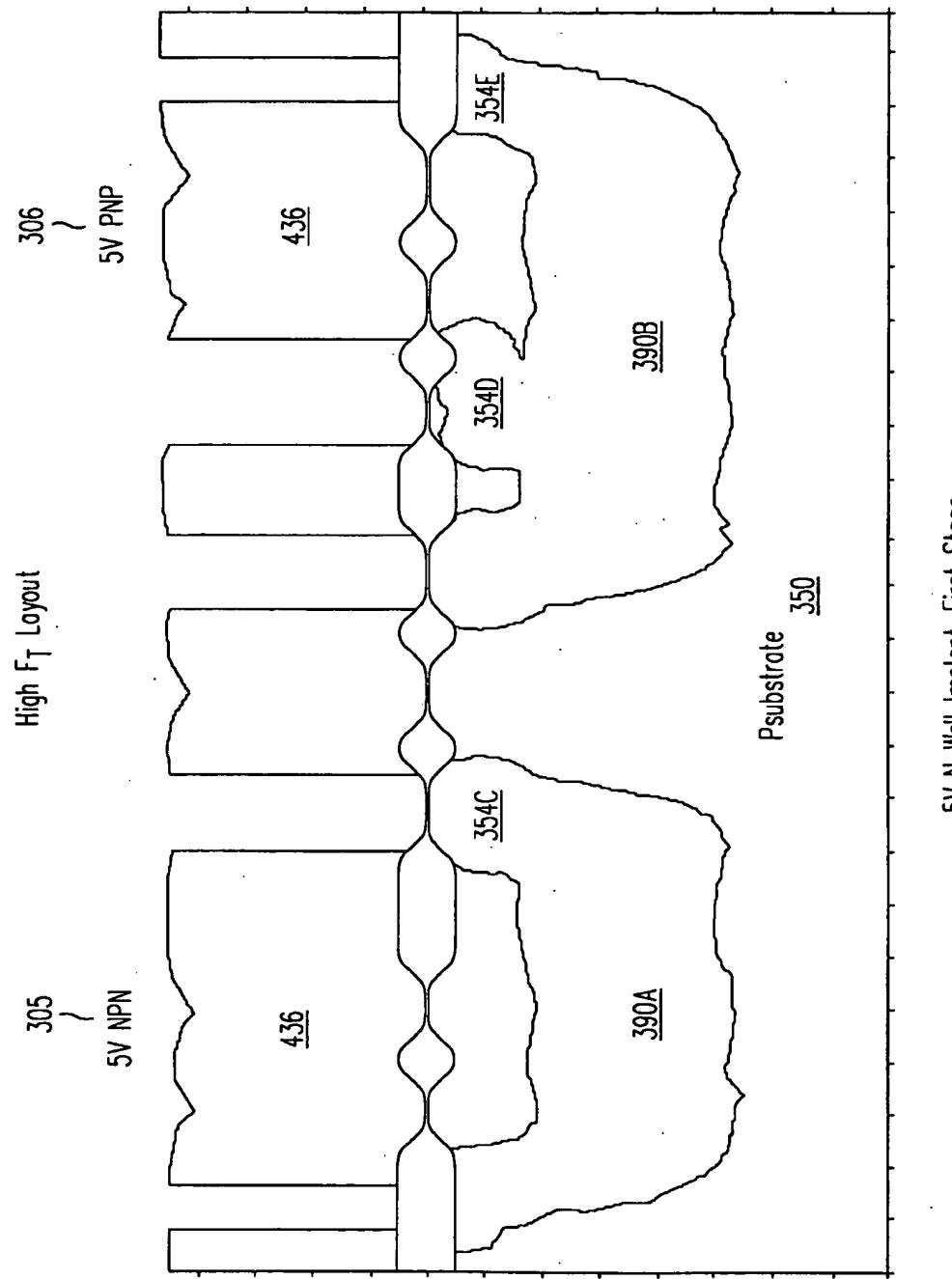


FIG. 40B

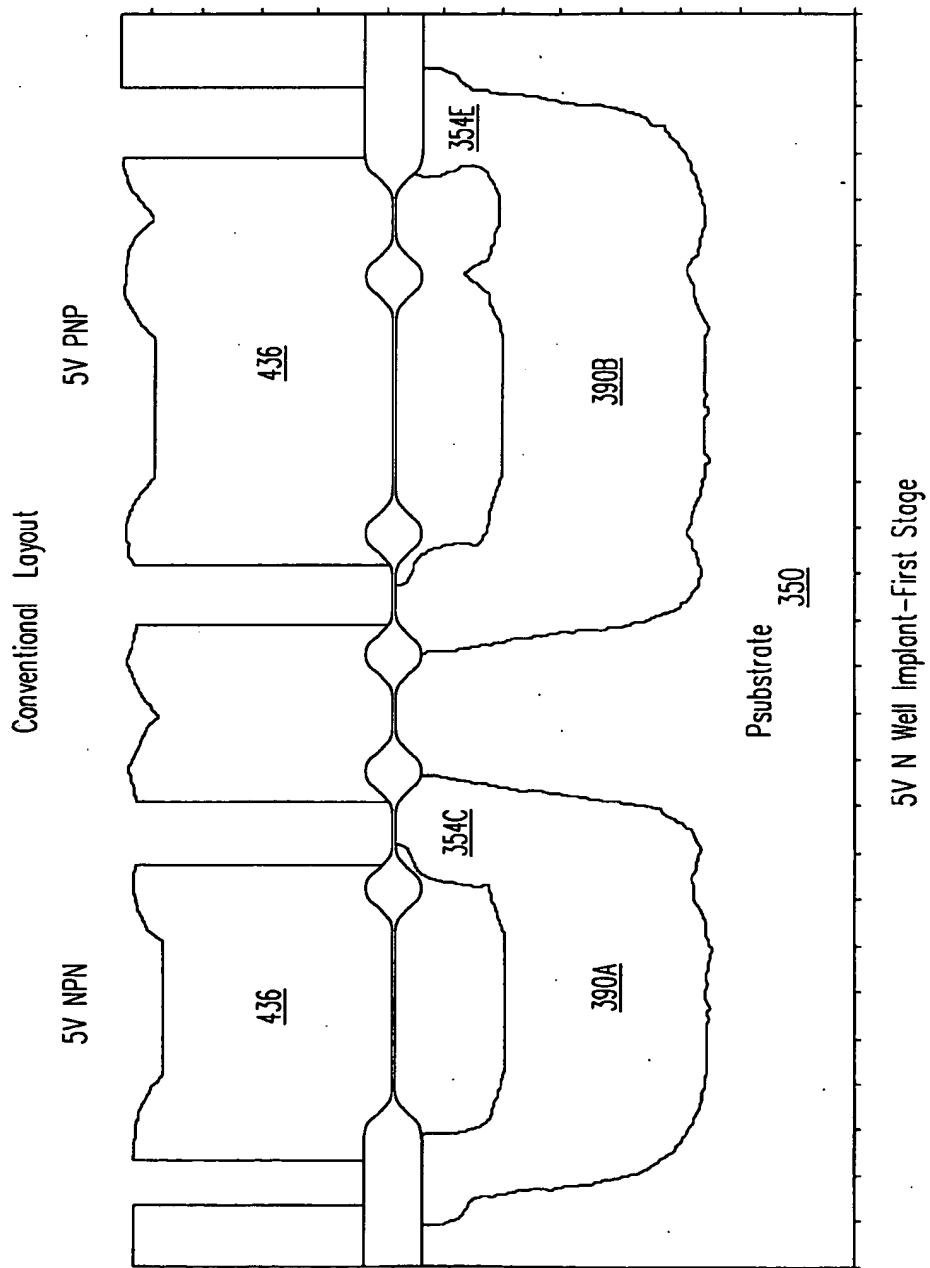
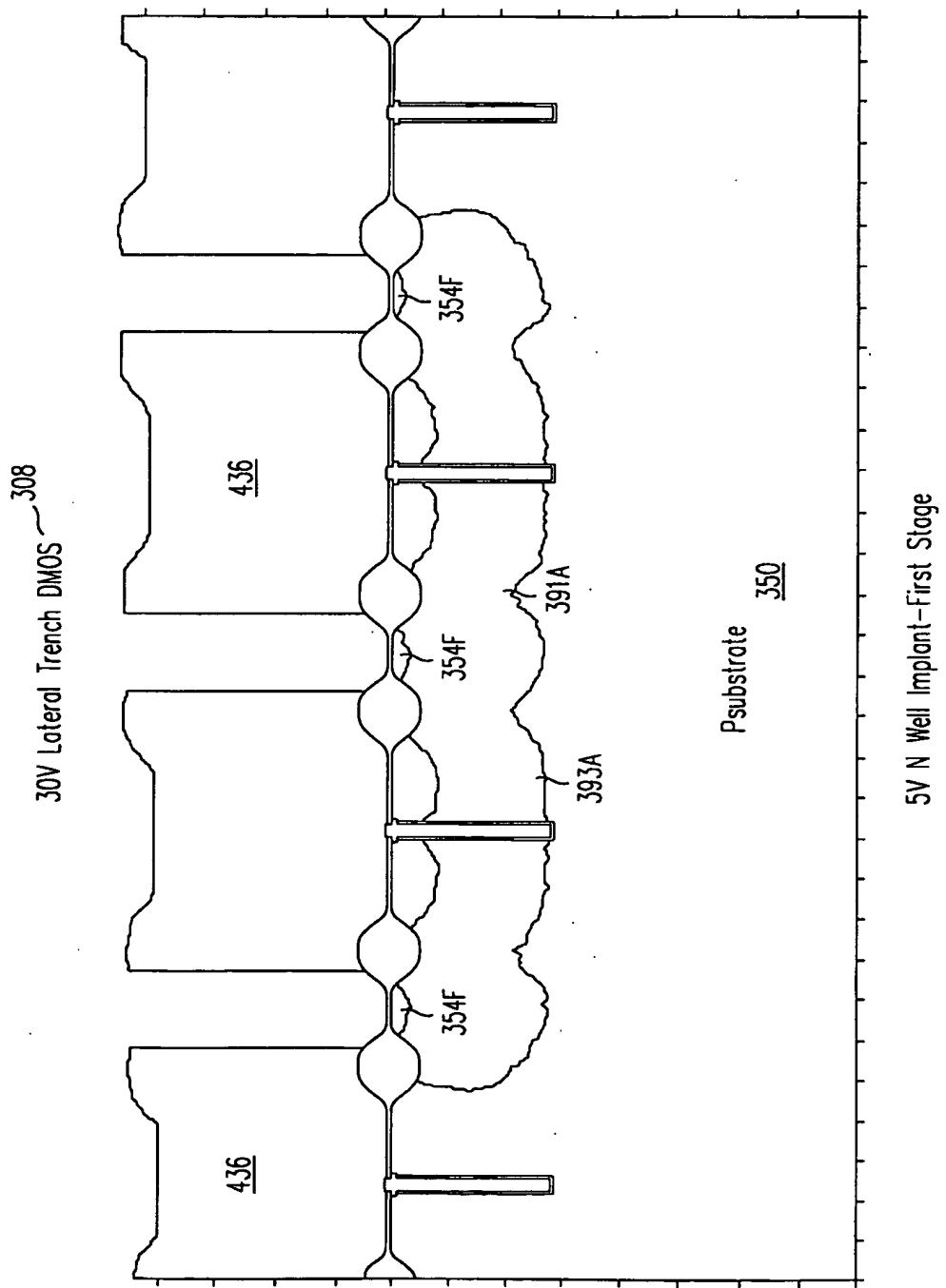


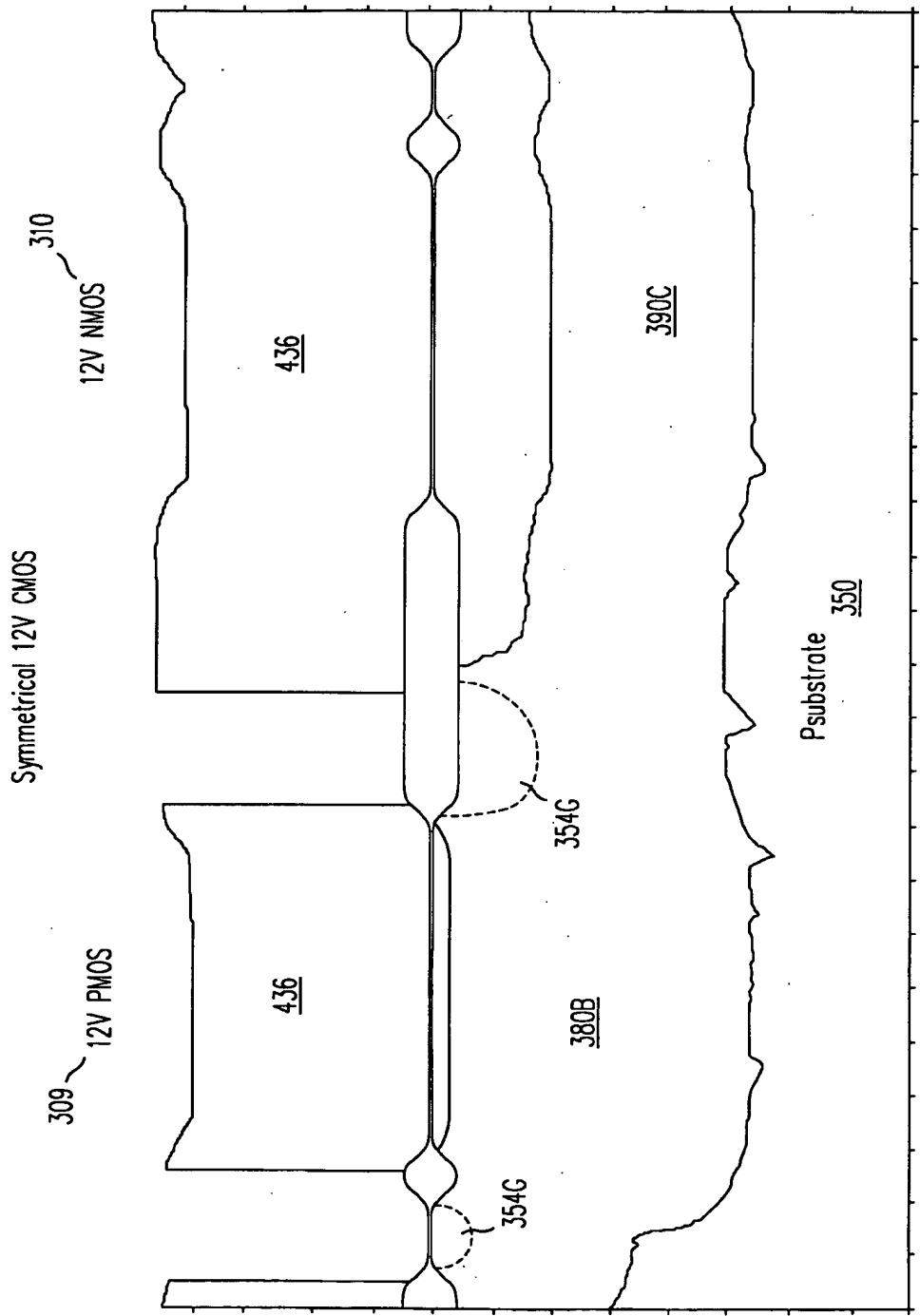
FIG. 40C

5V N Well Implant-First Stage

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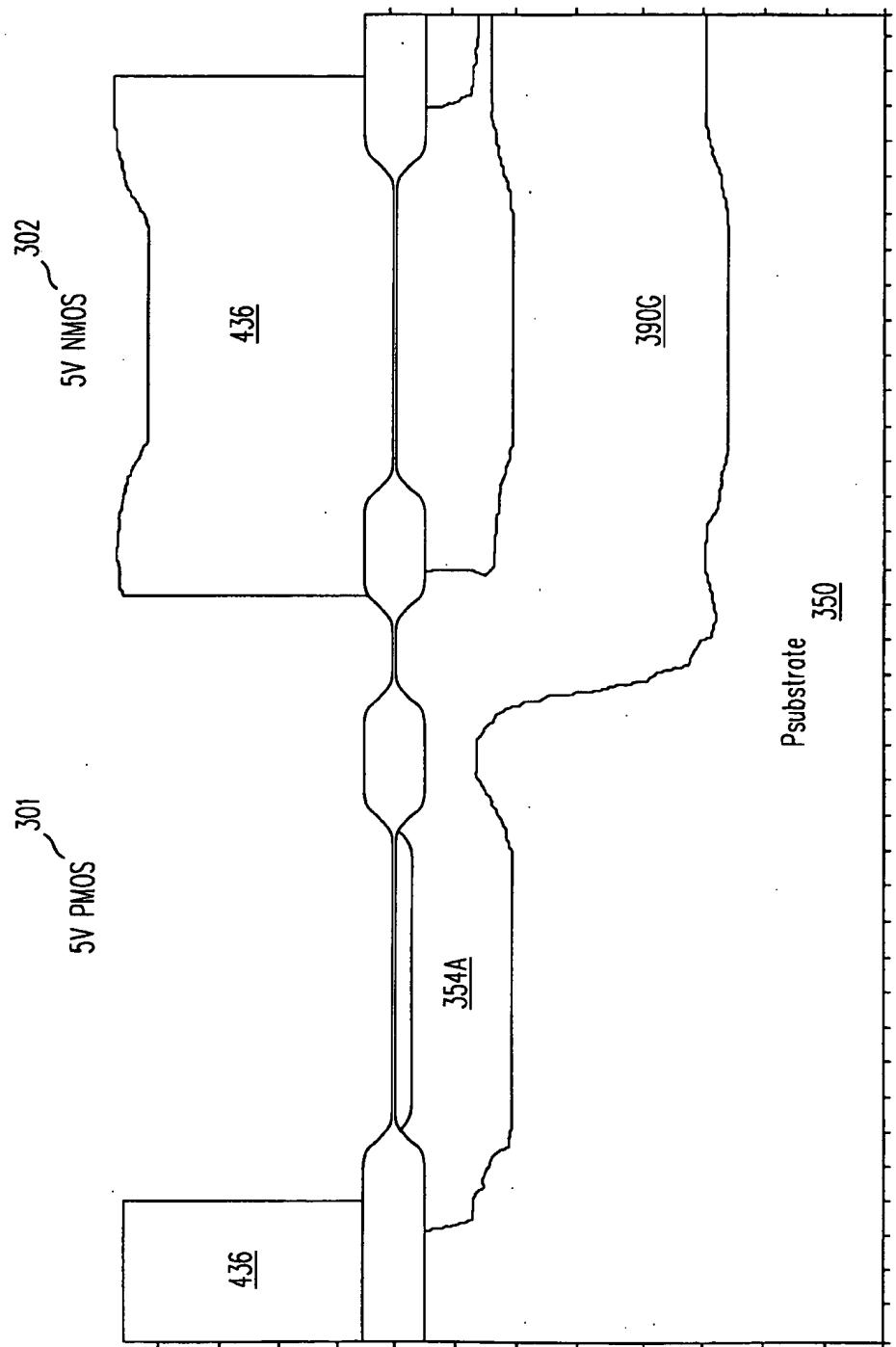
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5V N Well Implant-First Stage

FIG. 40E

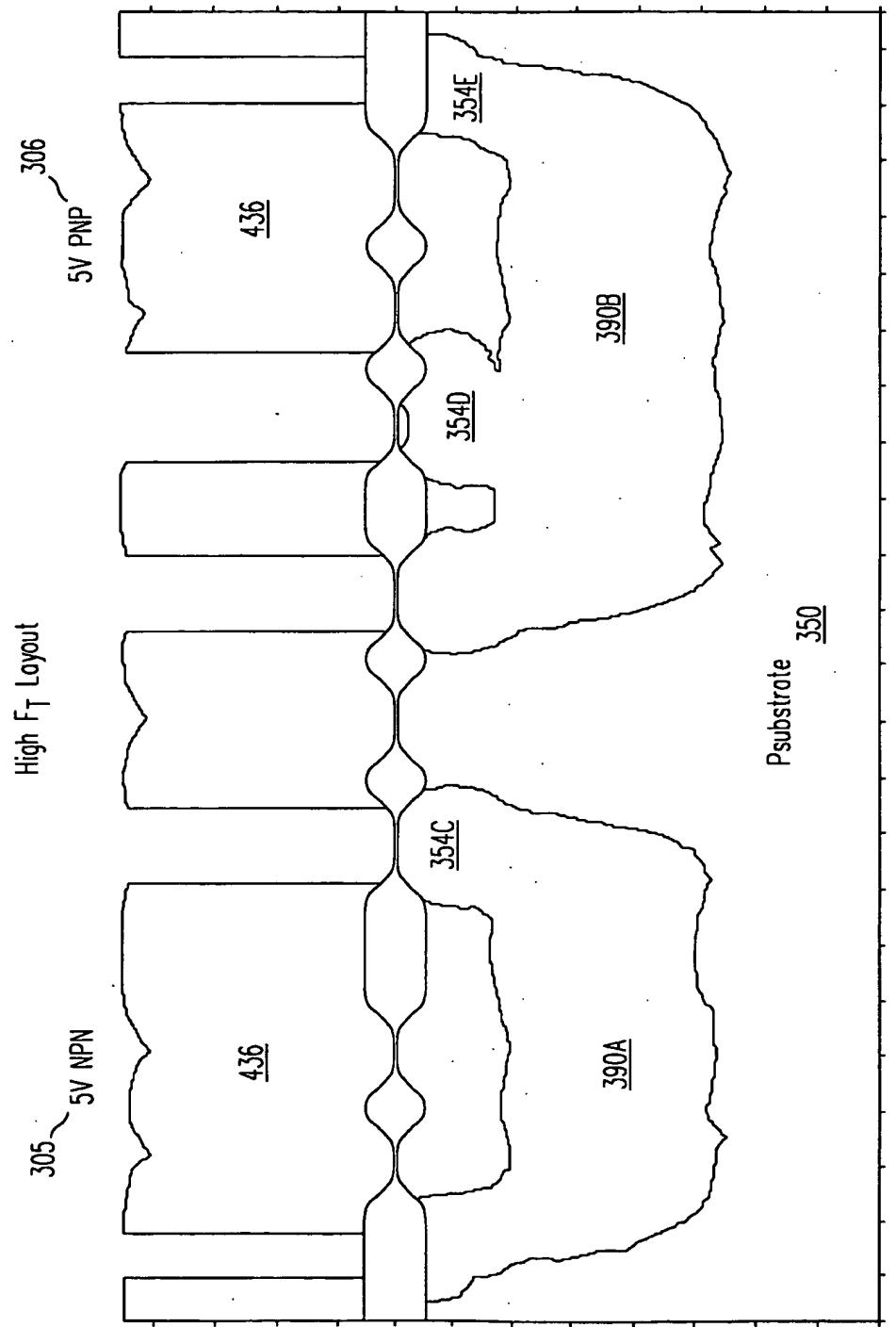
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5V N Well Implant - Second Stage

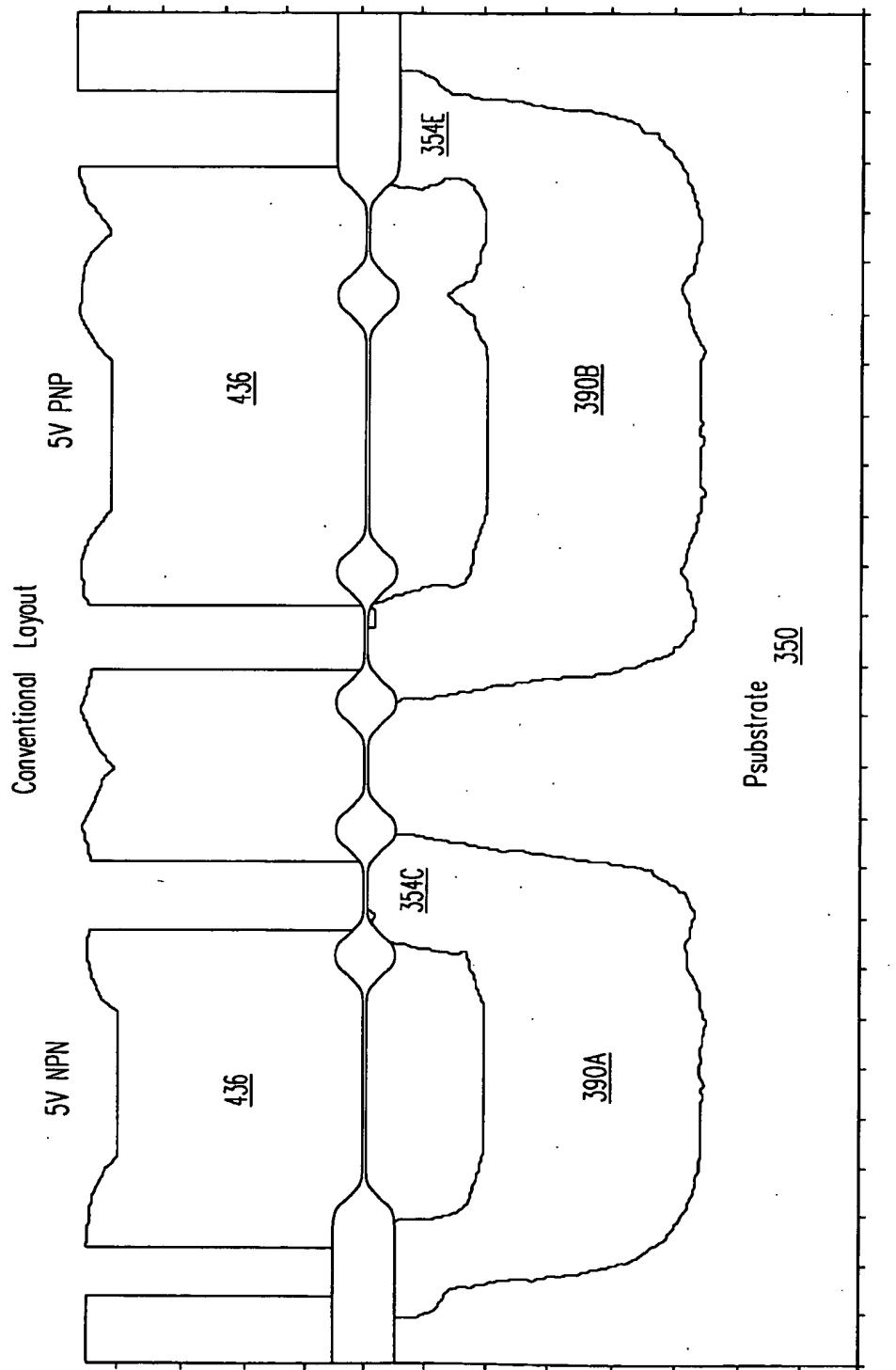
FIG. 41A

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5V N Well Implant - Second Stage

FIG. 41B



5V N Well Implant - Second Stage

FIG. 41C

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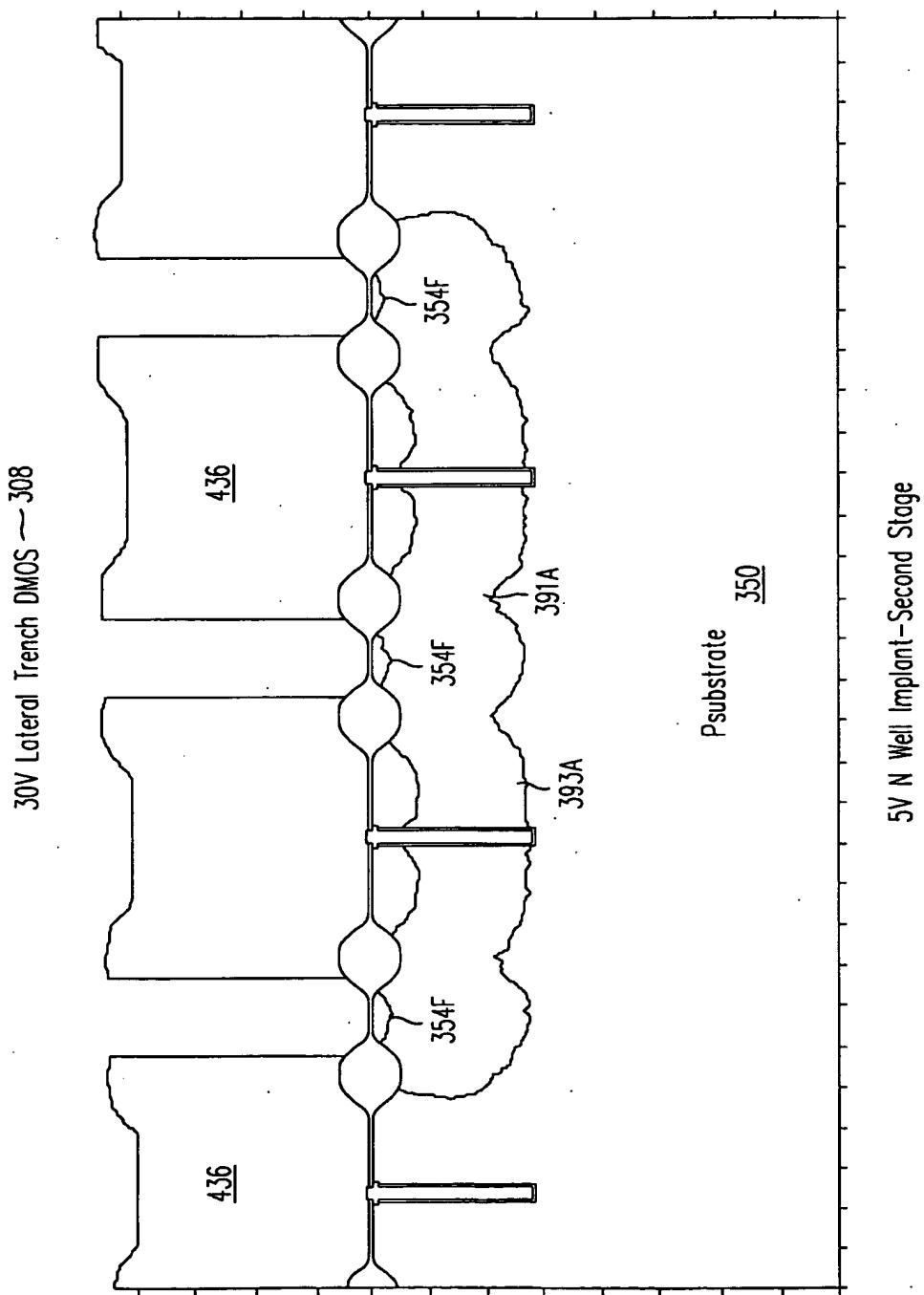
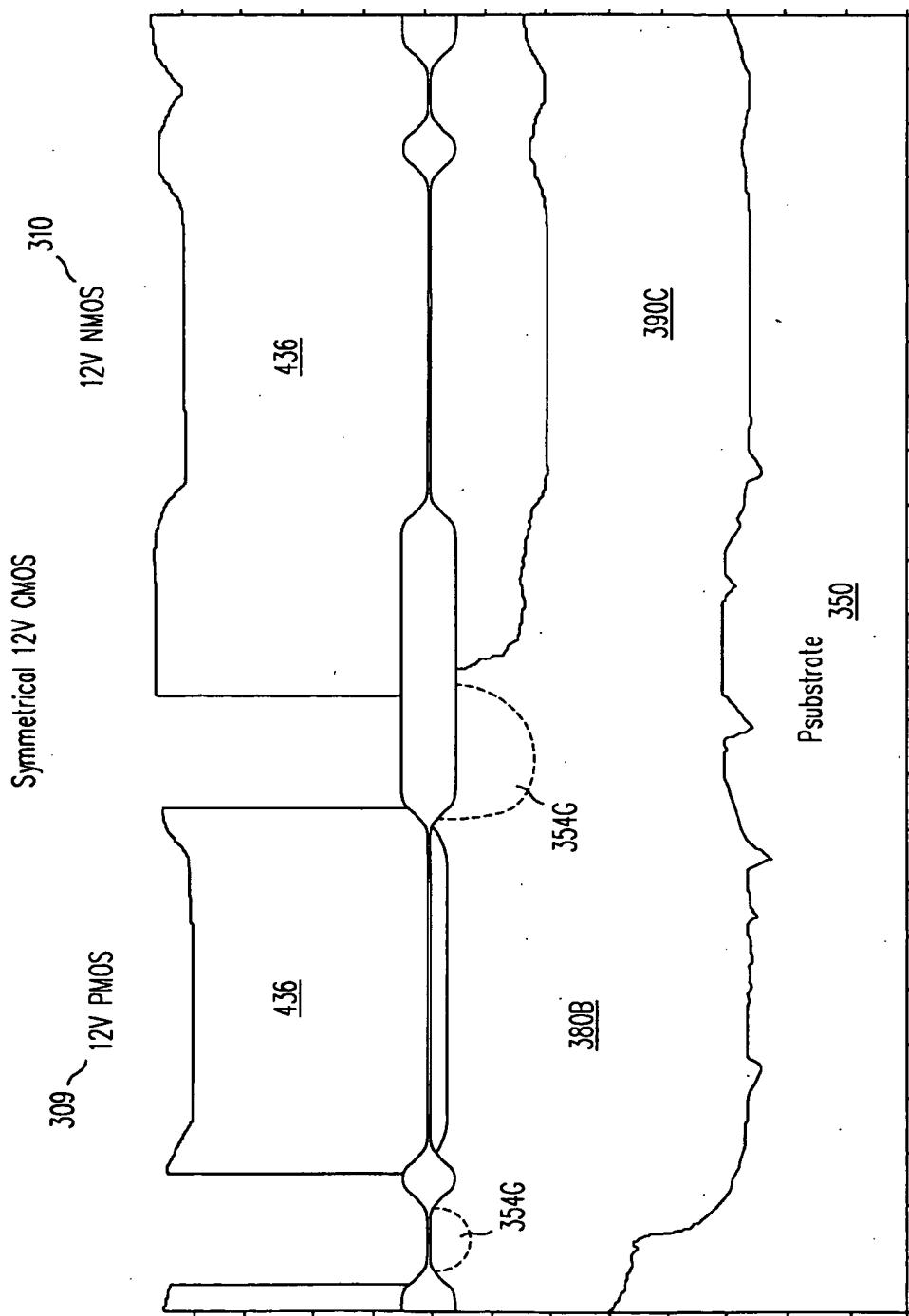


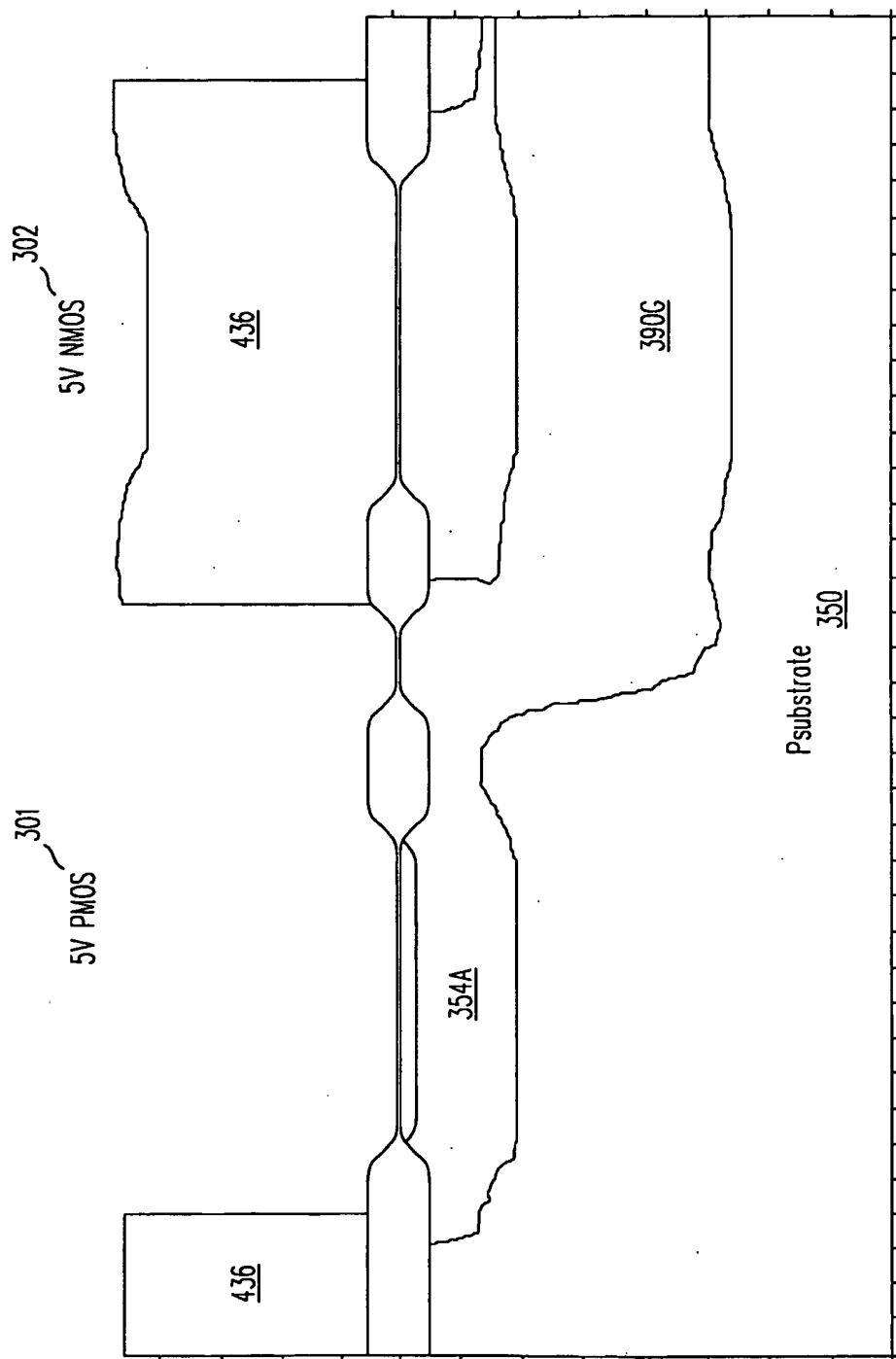
FIG. 41D



5V N Well Implant - Second Stage

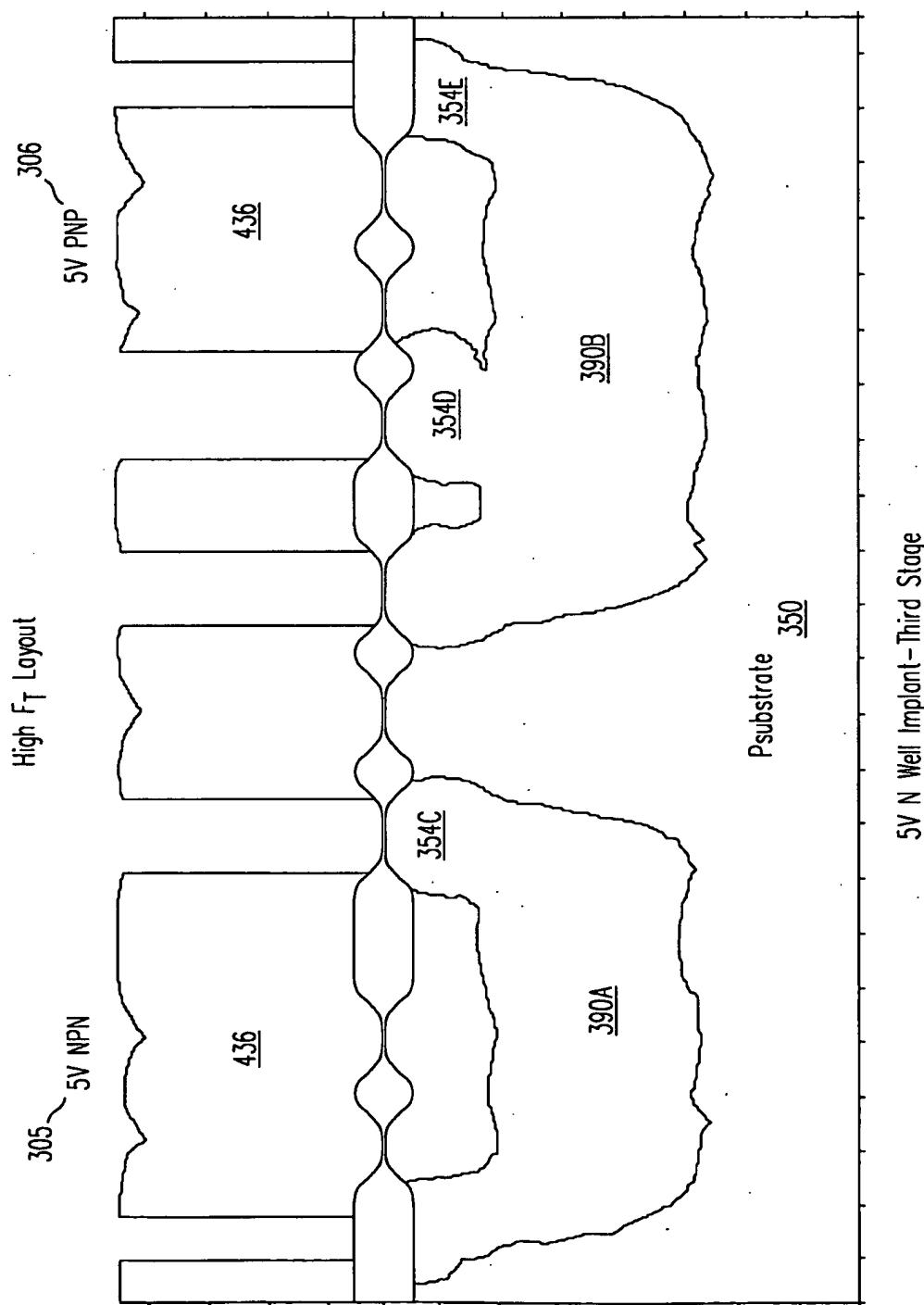
FIG. 41E

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5V N Well Implant-Third Stage

FIG. 42A



5V N Well Implant-Third Stage

FIG. 42B

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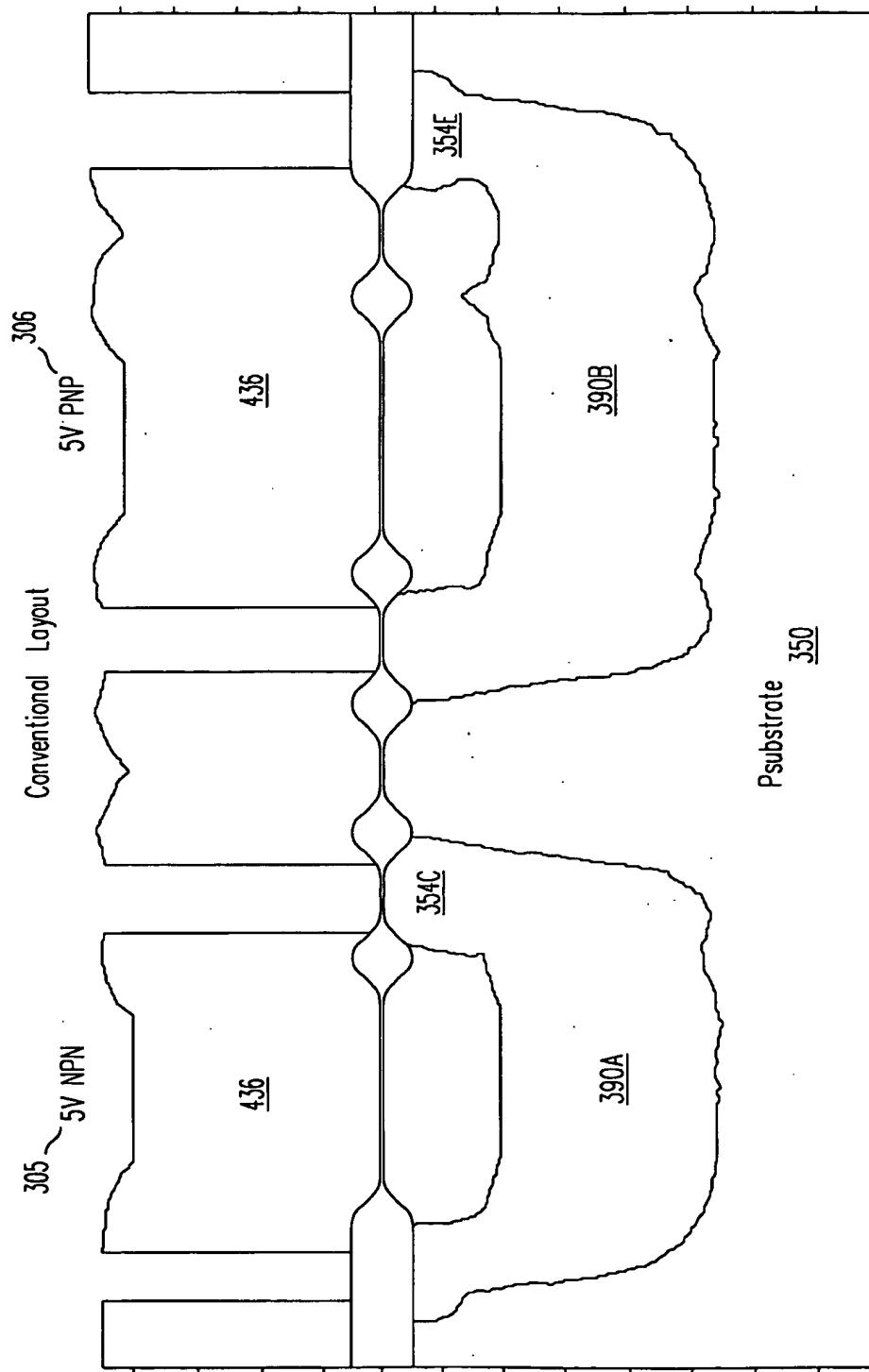
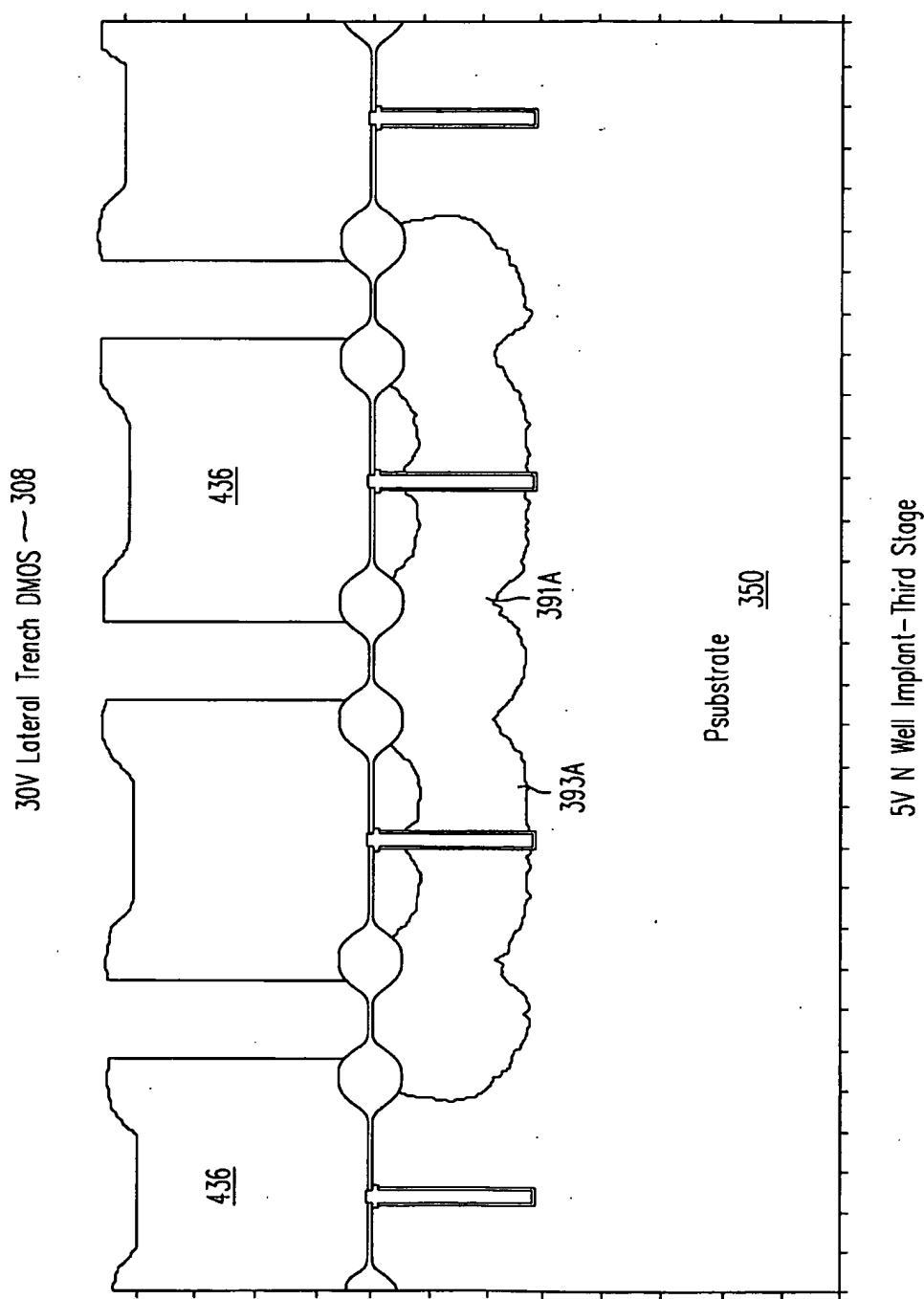
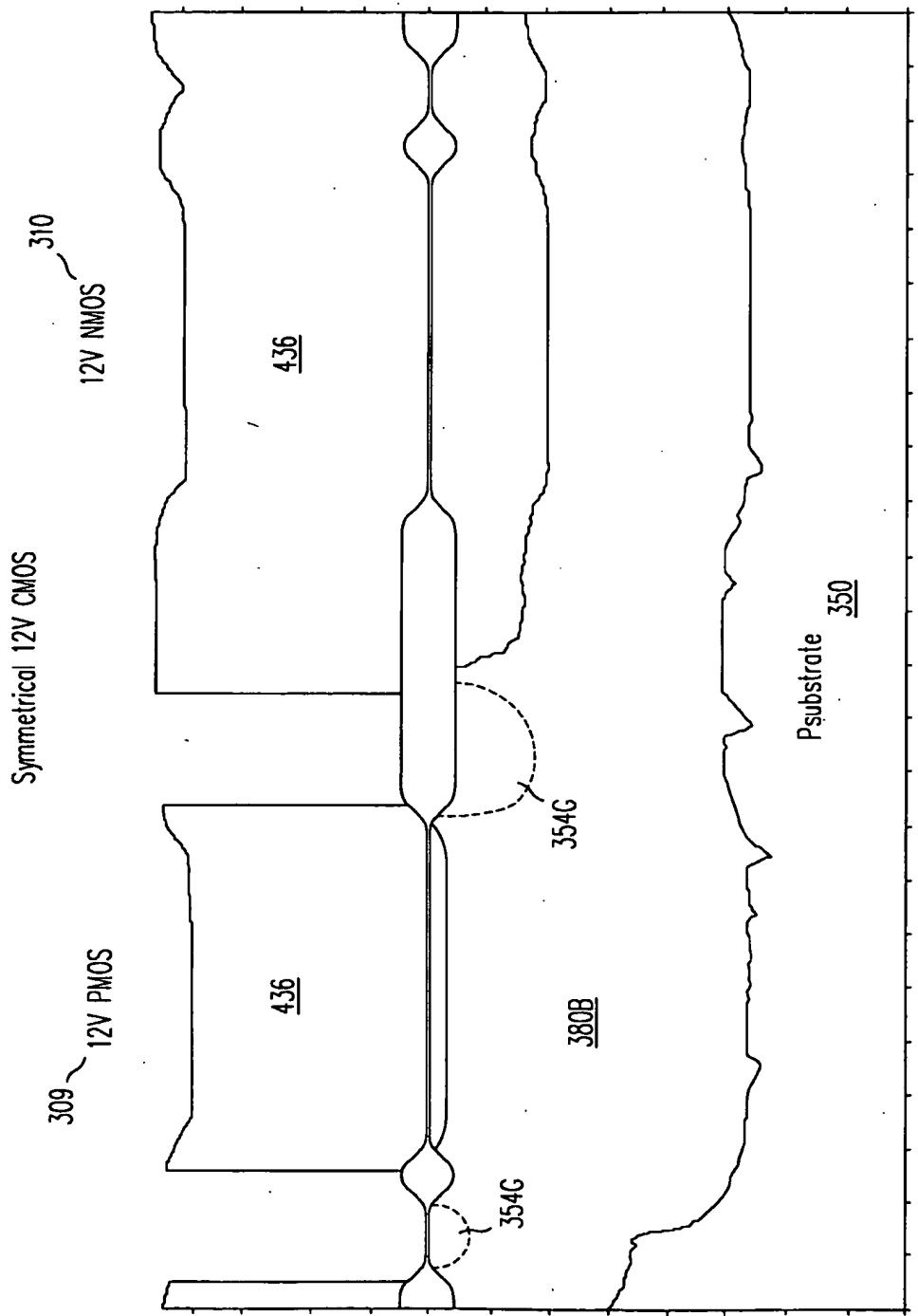


FIG. 42C



5V N Well Implant - Third Stage

FIG. 42D



5V N Well implant - Third Stage

FIG. 42E

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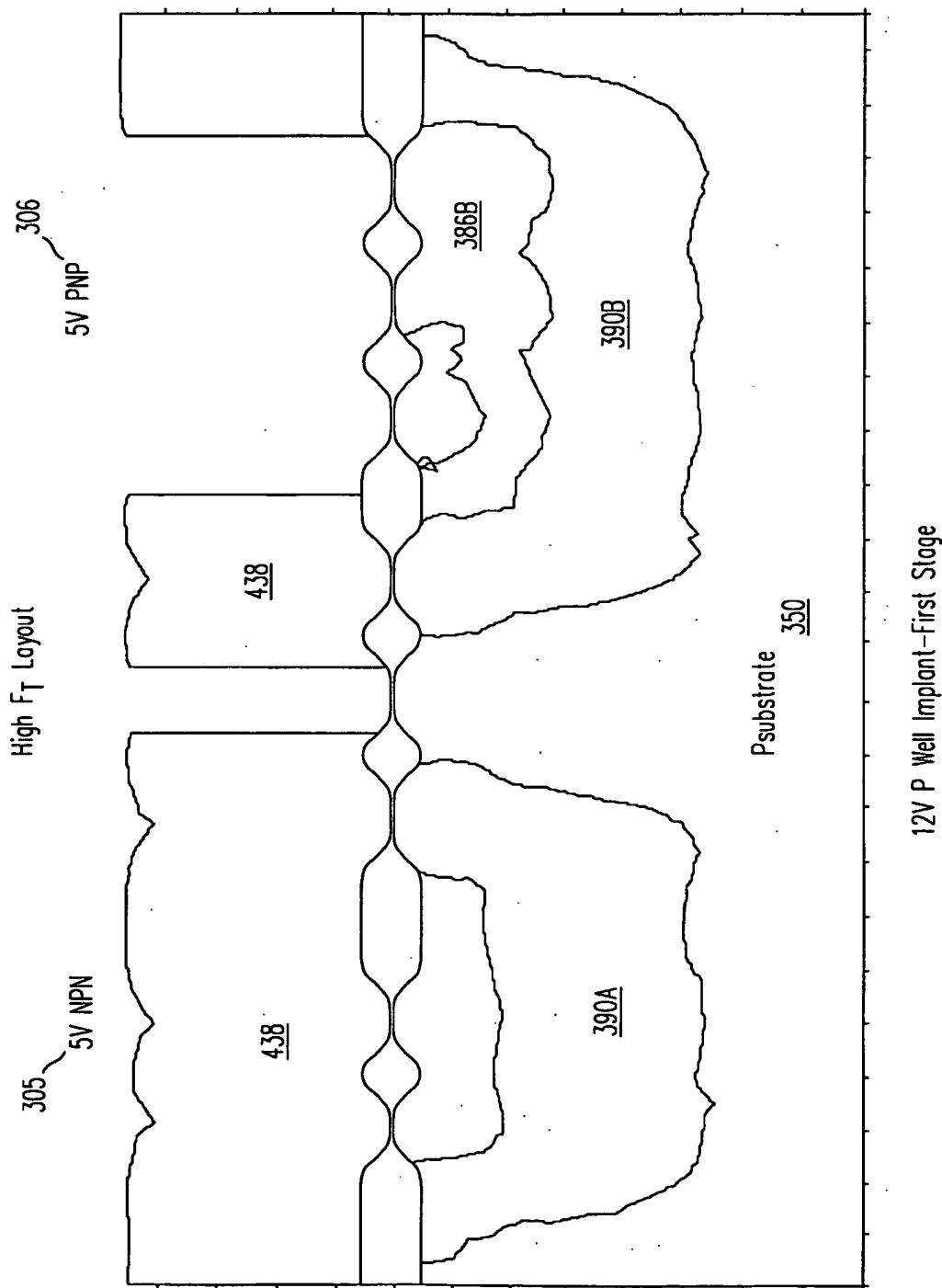


FIG. 43B

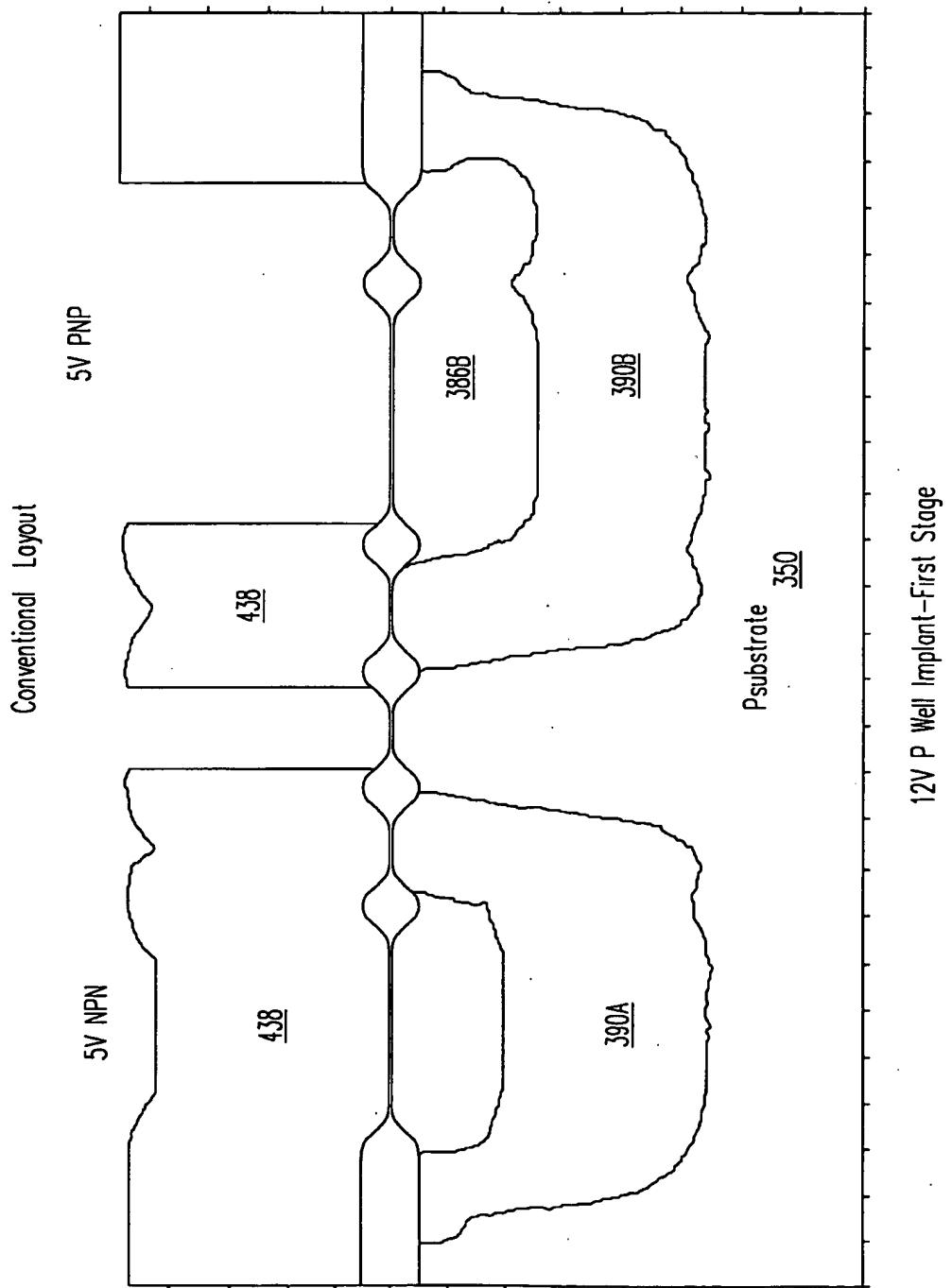
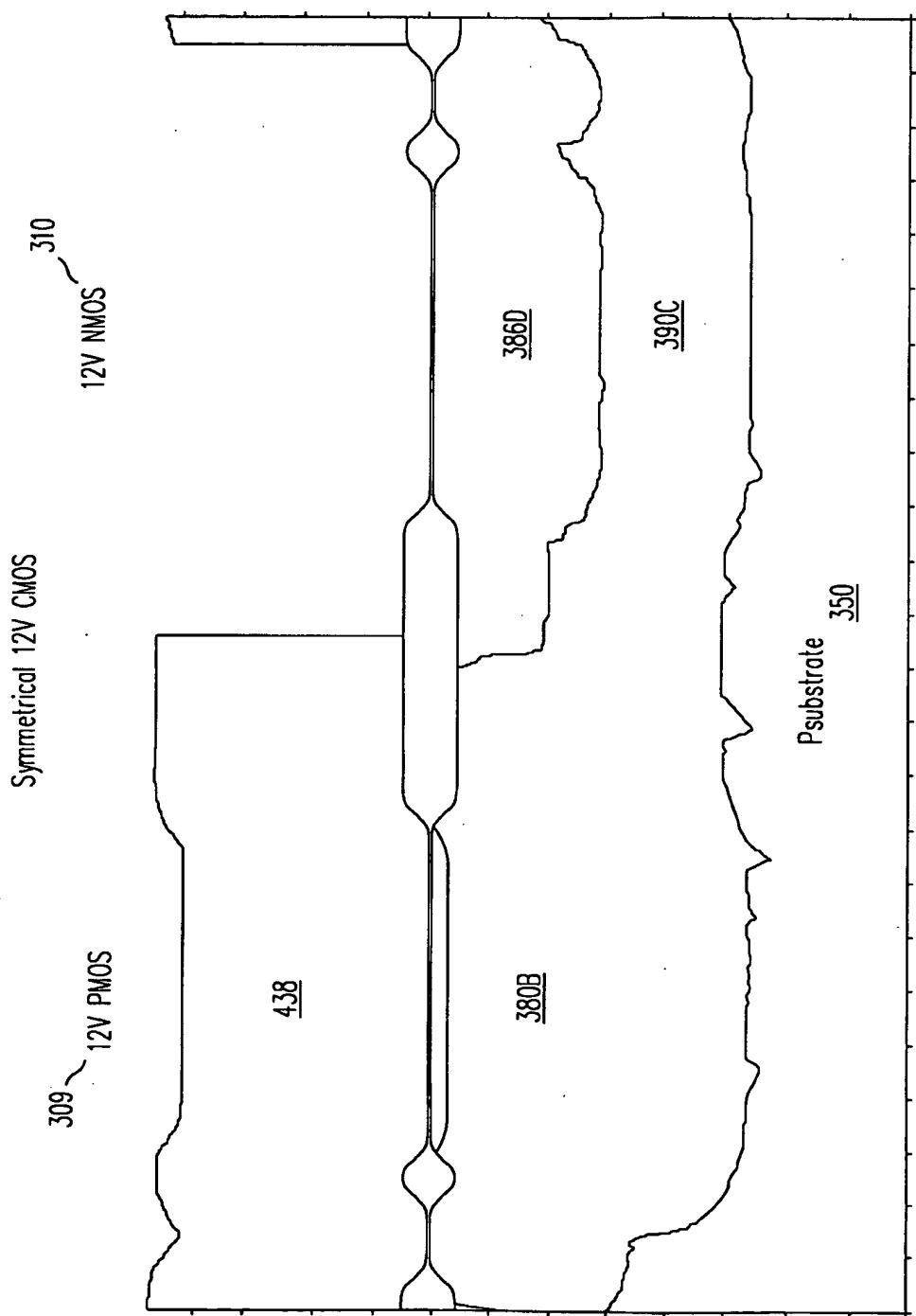


FIG. 43C



12V P Well Implant - First Stage

FIG. 43E

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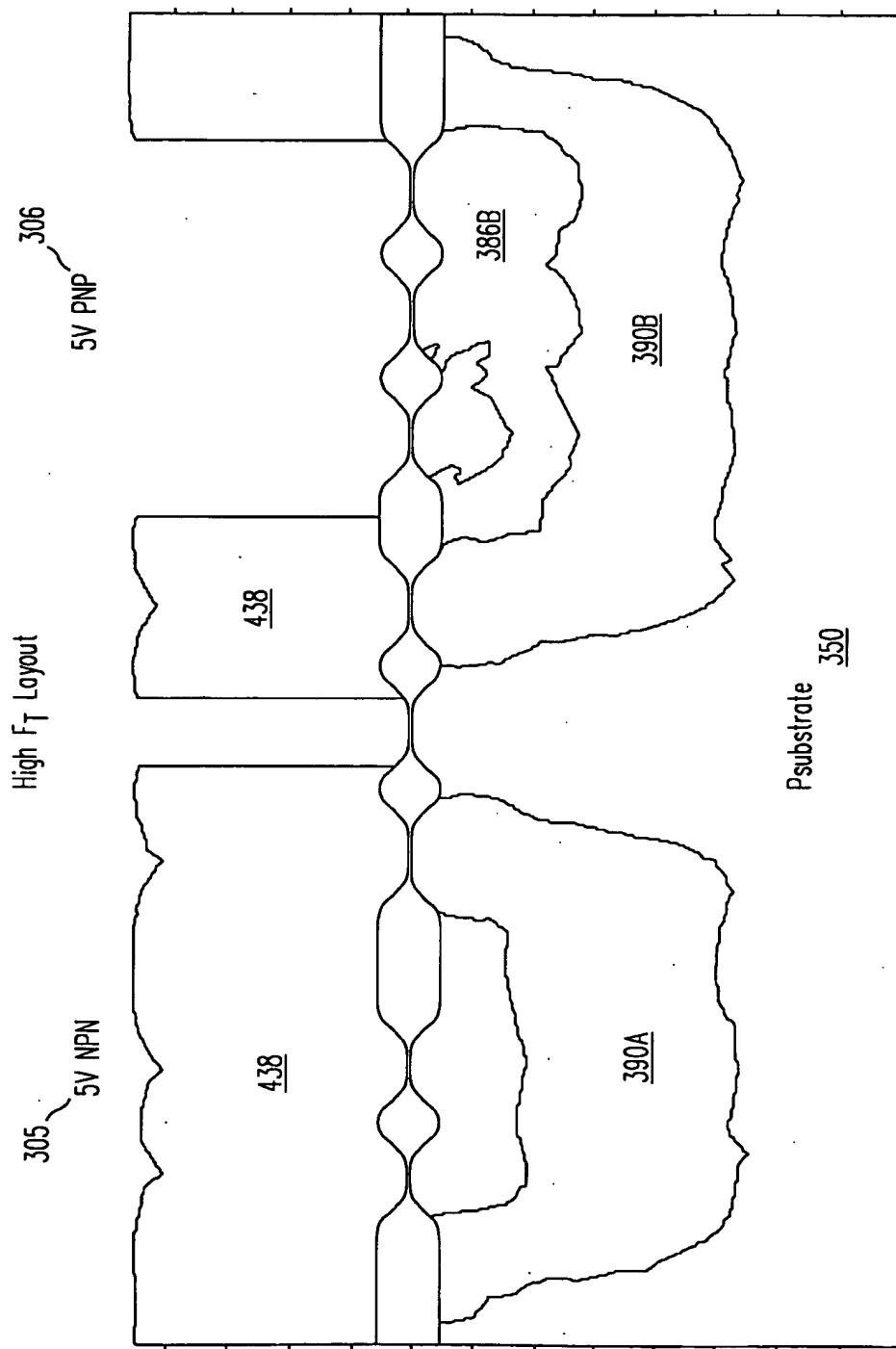
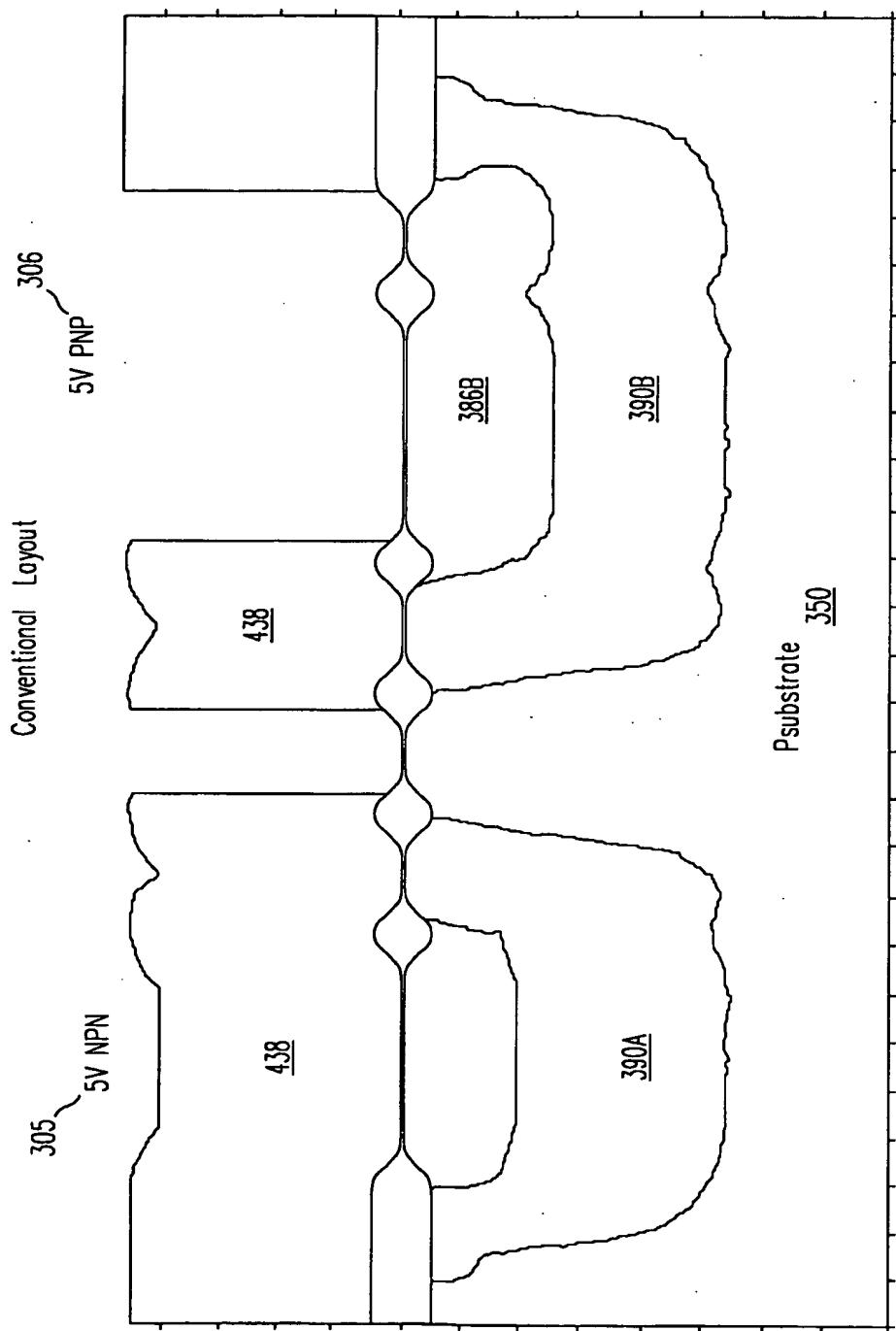


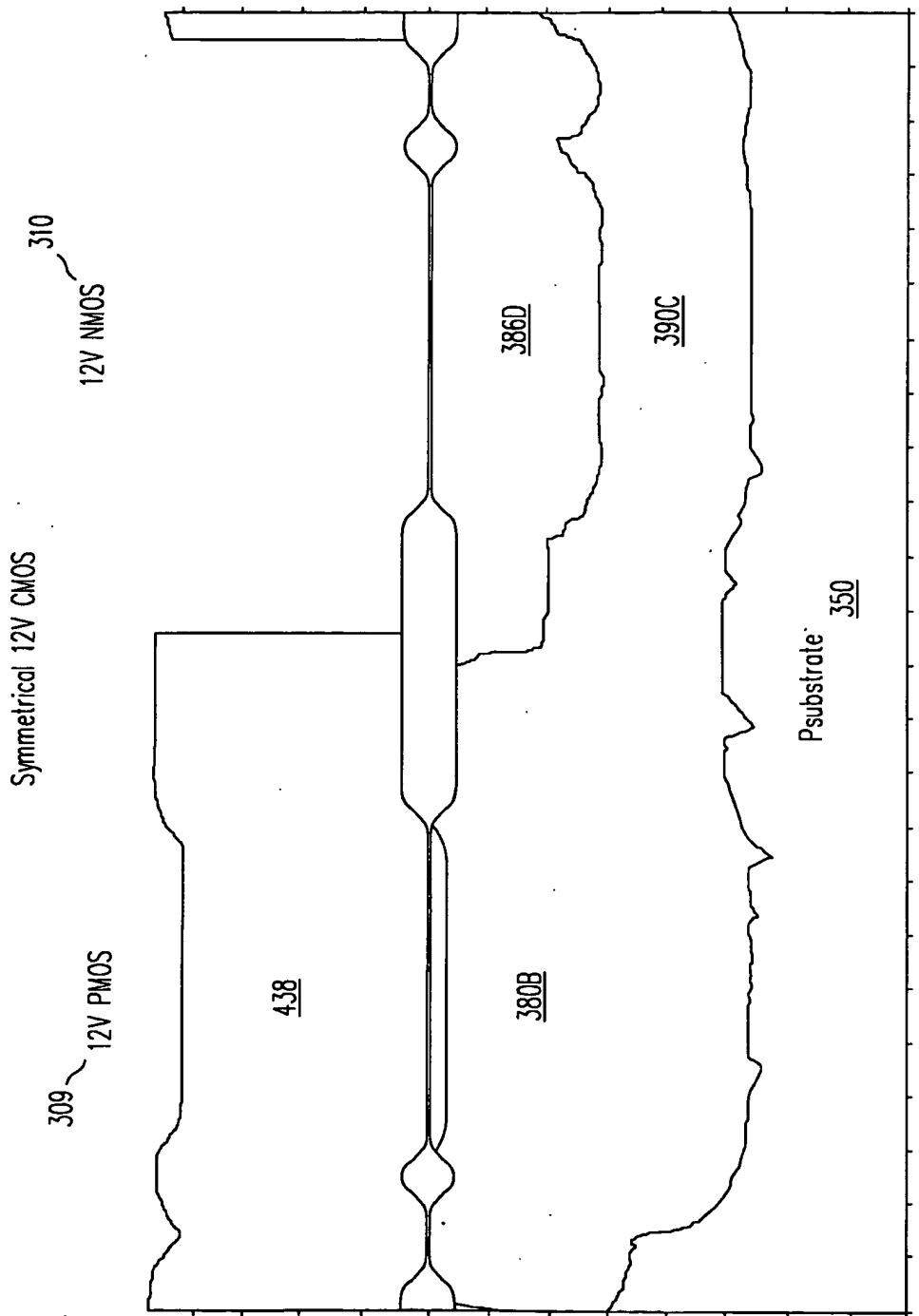
FIG. 44B



12V P Well Implant-Second Stage

FIG. 44C

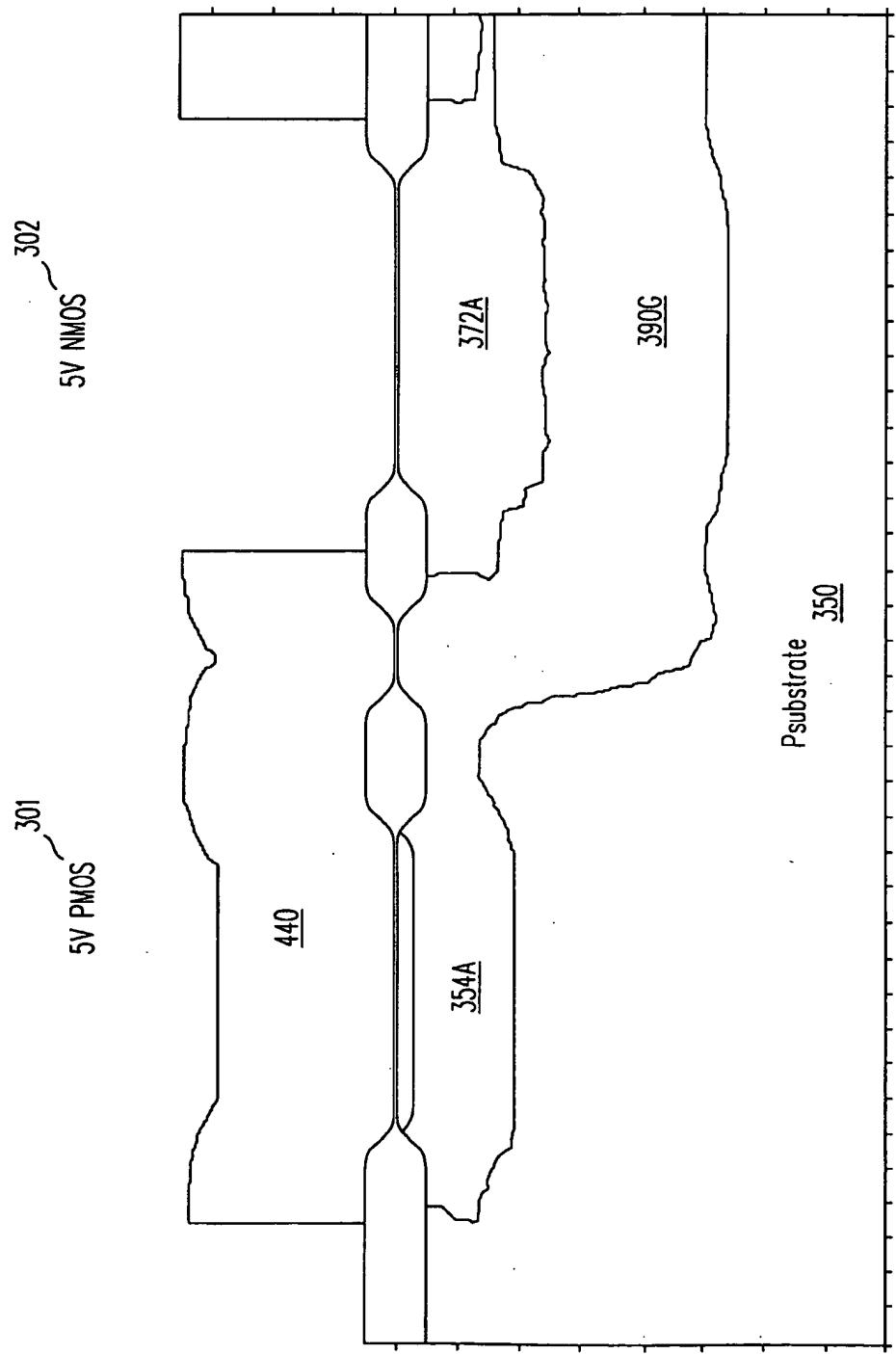
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12V P Well Implant—Second Stage

FIG. 44E

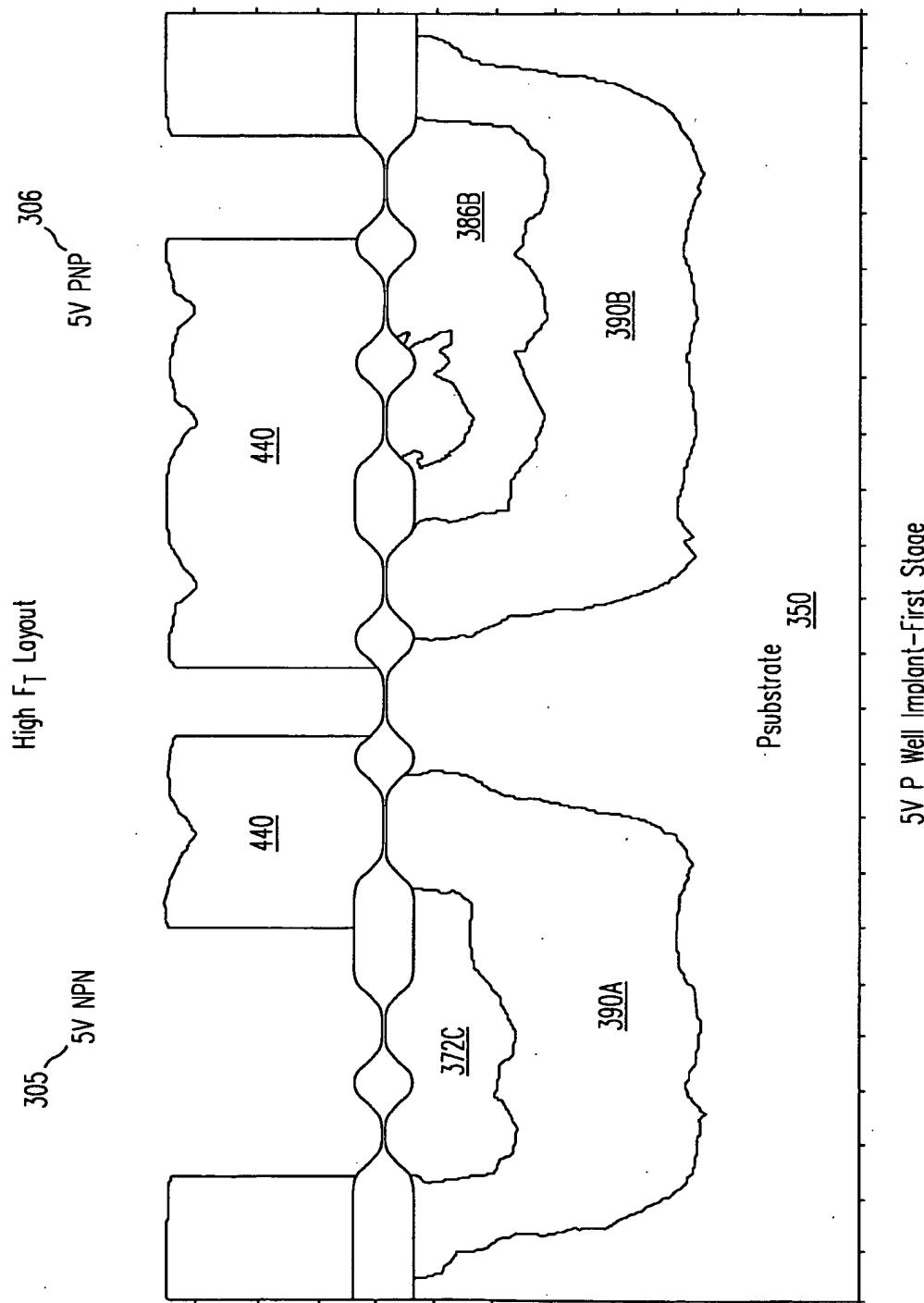
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5V P Well Implant-First Stage

FIG. 45A

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5V P Well Implant-First Stage

FIG. 45B

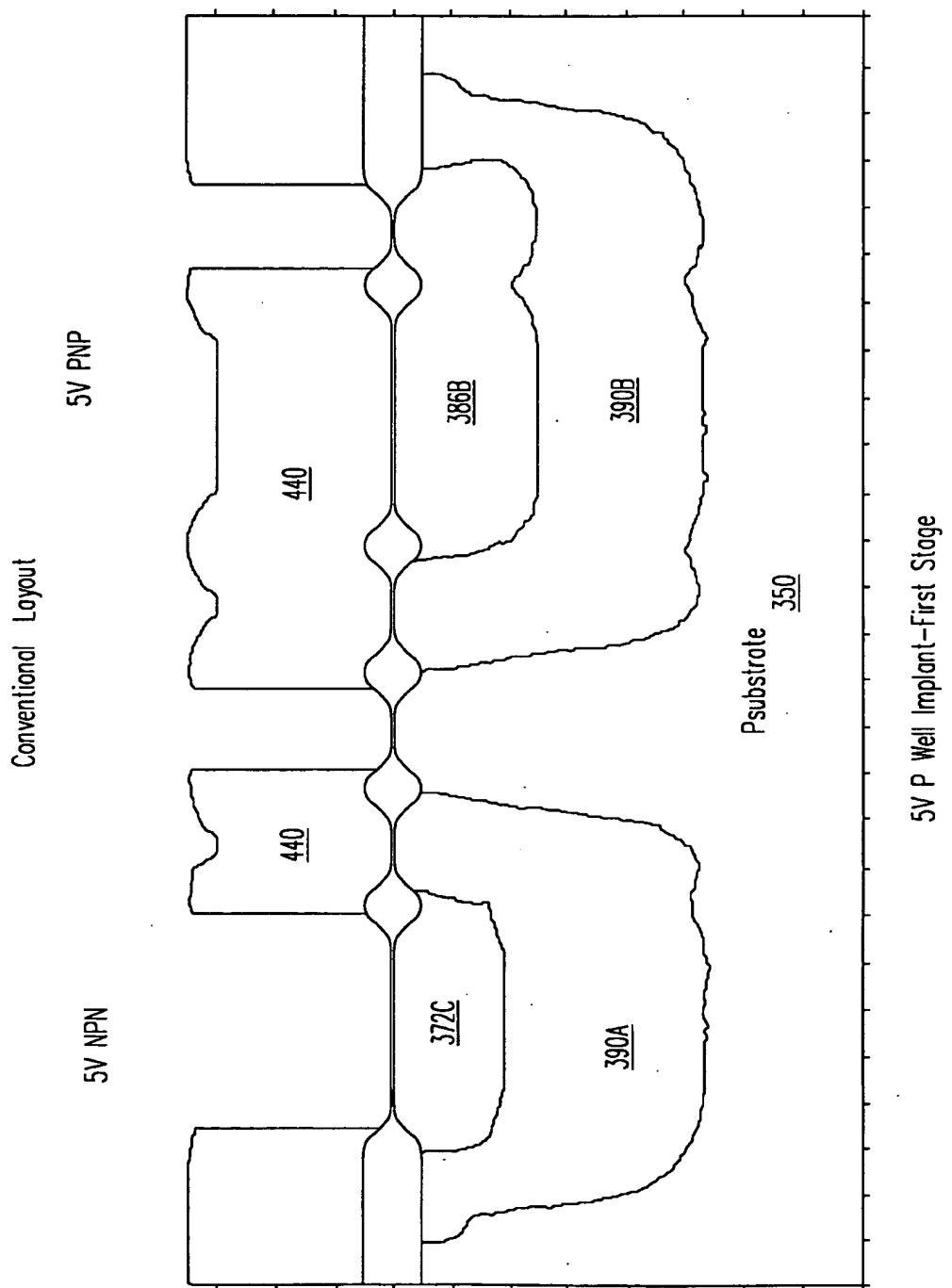
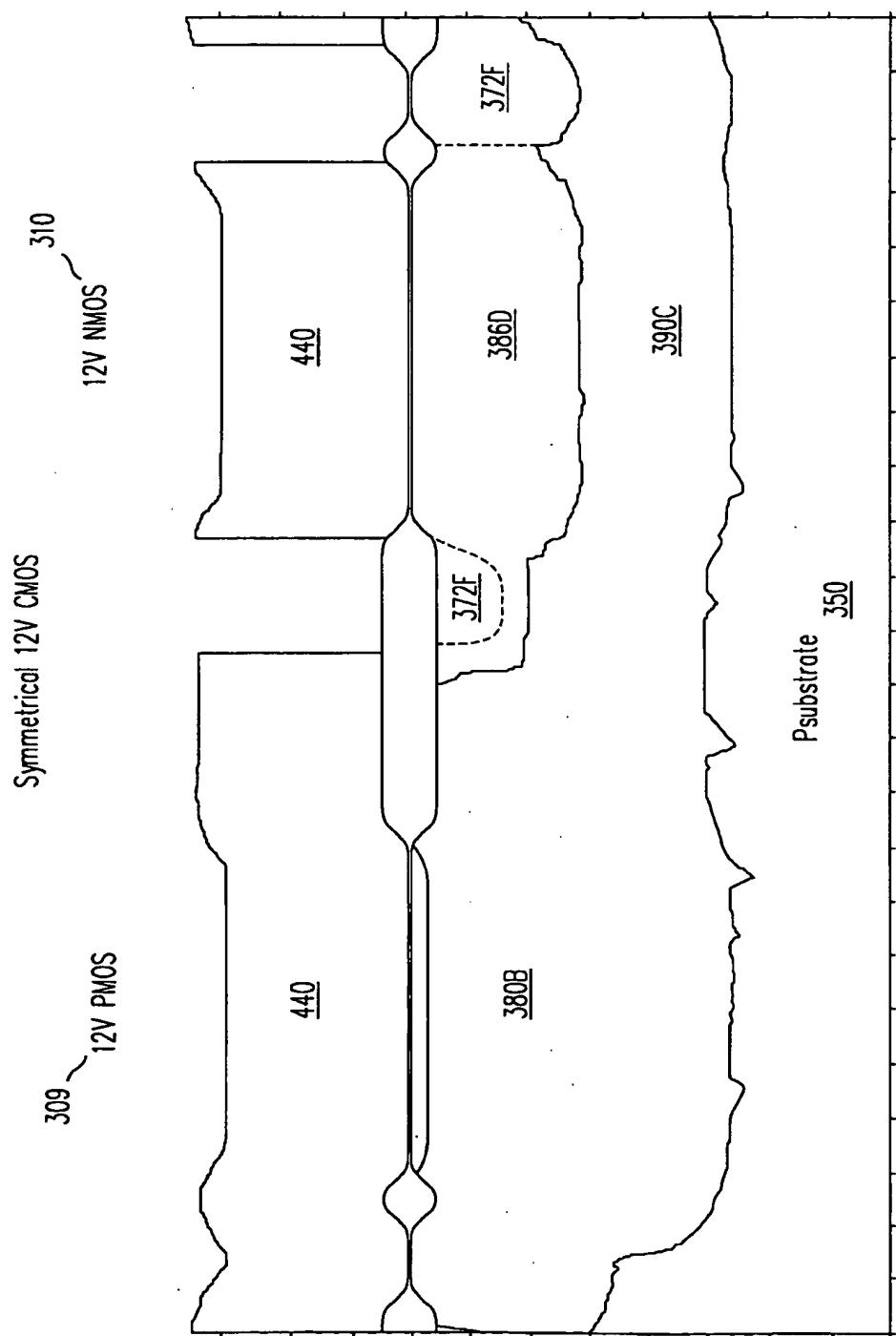


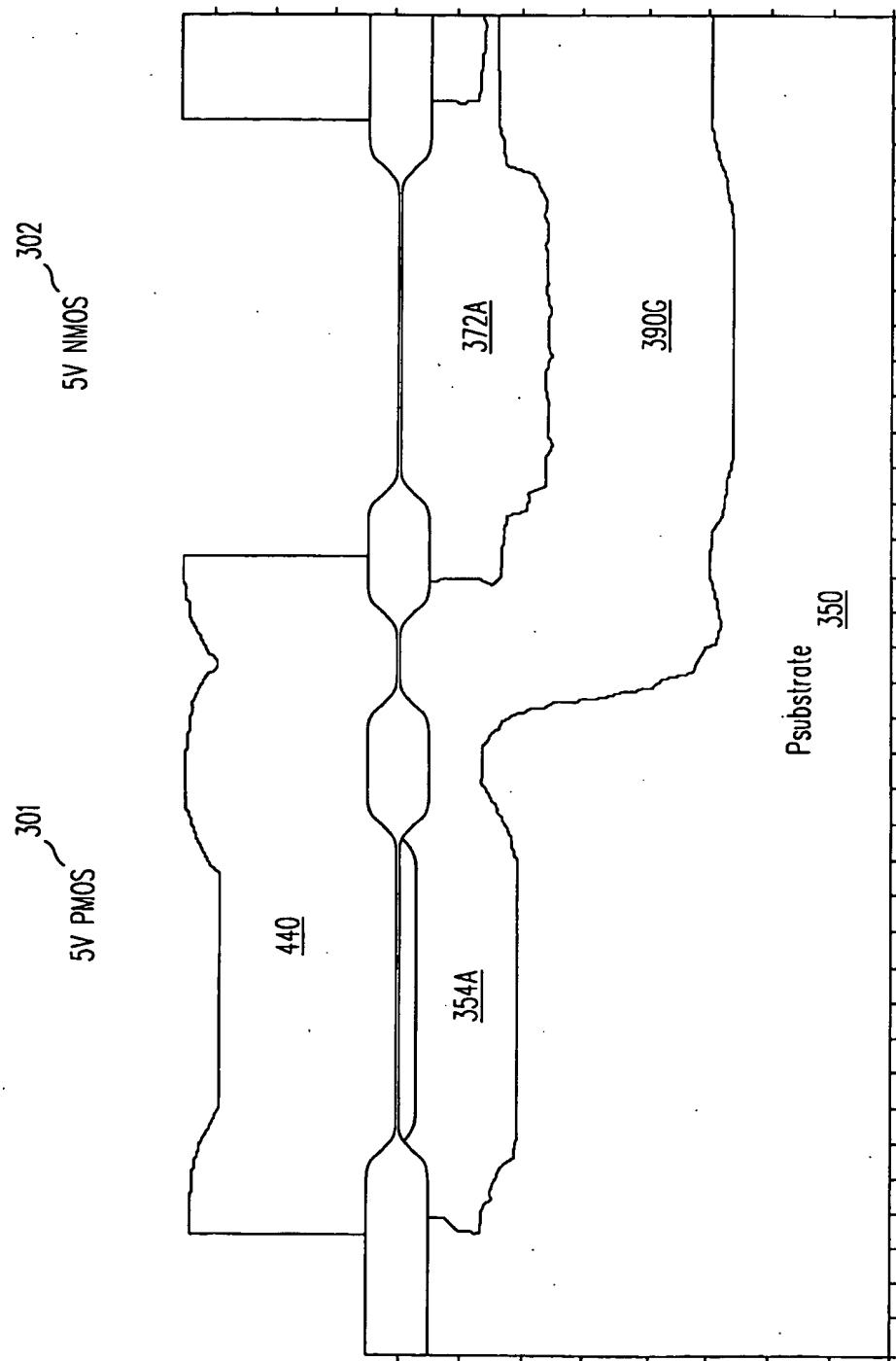
FIG. 45C



5V P Well Implant-First Stage

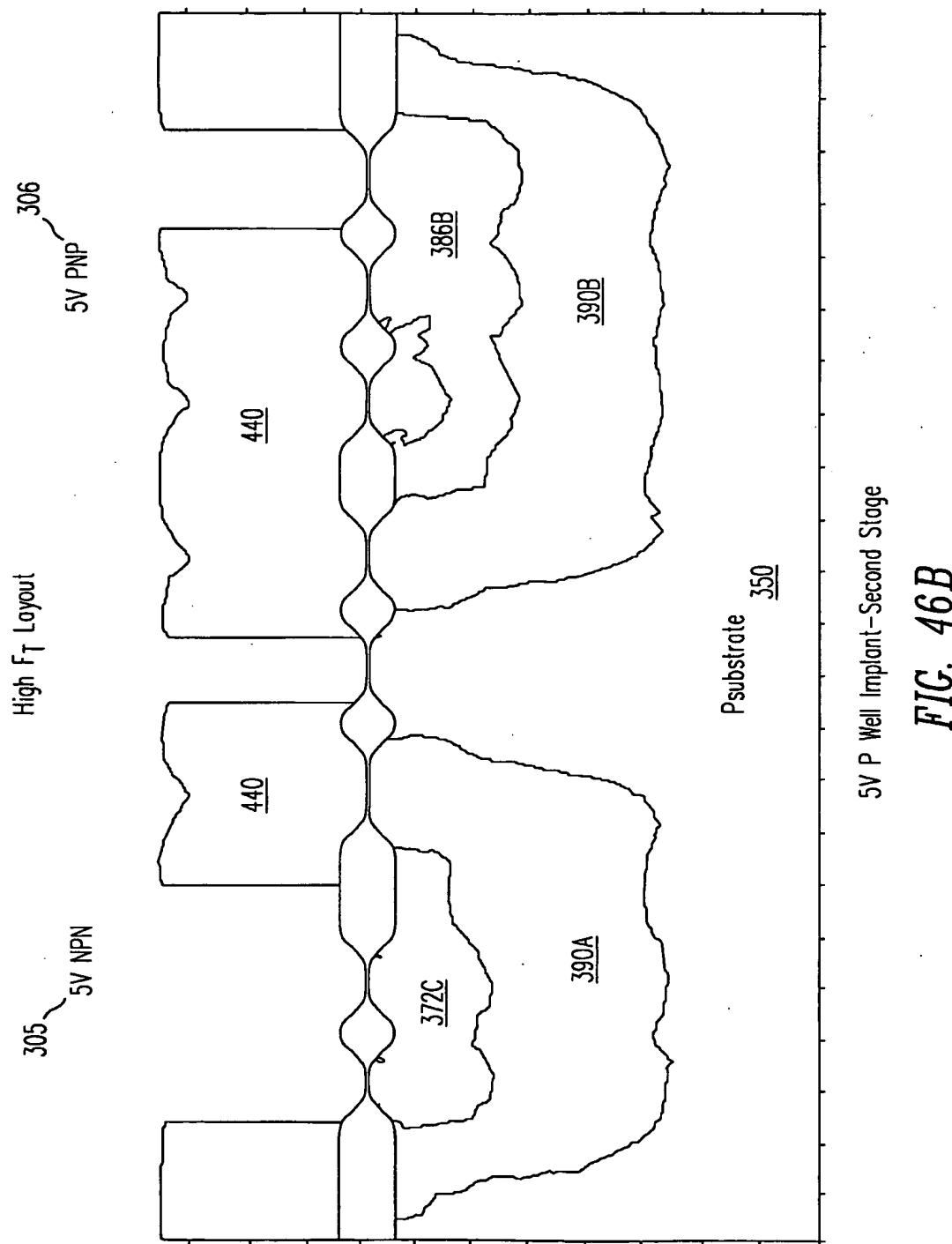
FIG. 45E

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5V P Well Implant - Second Stage

FIG. 46A



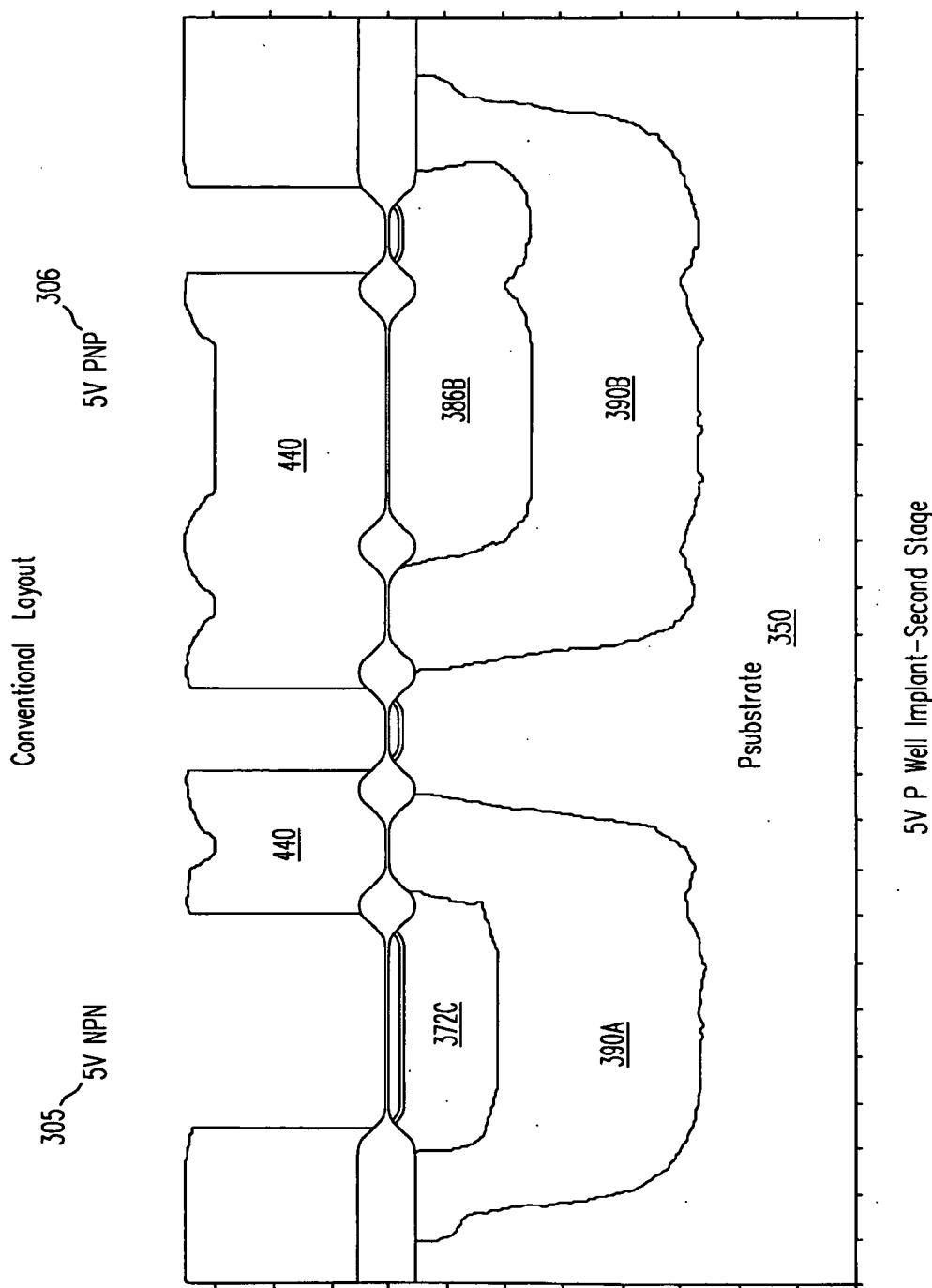
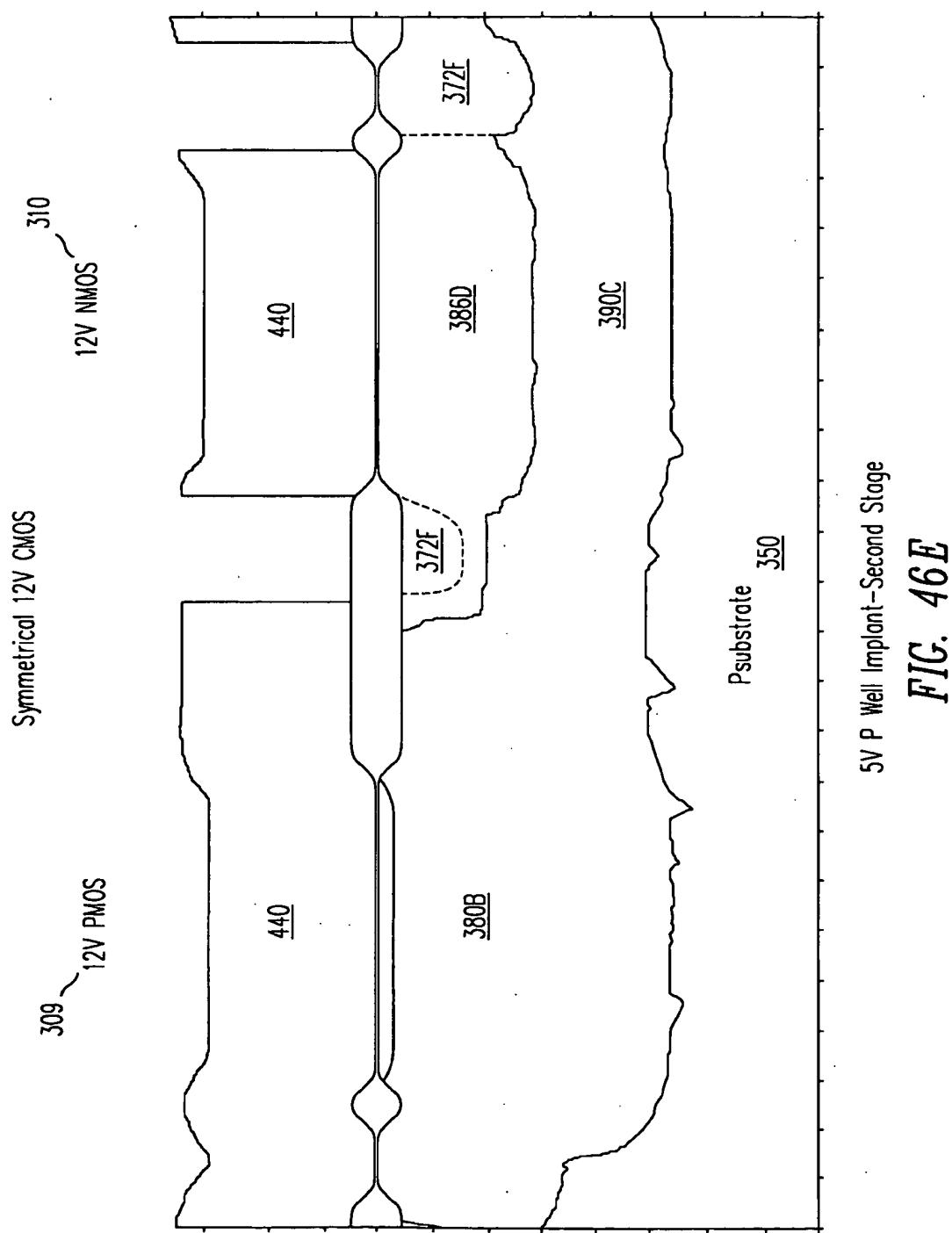


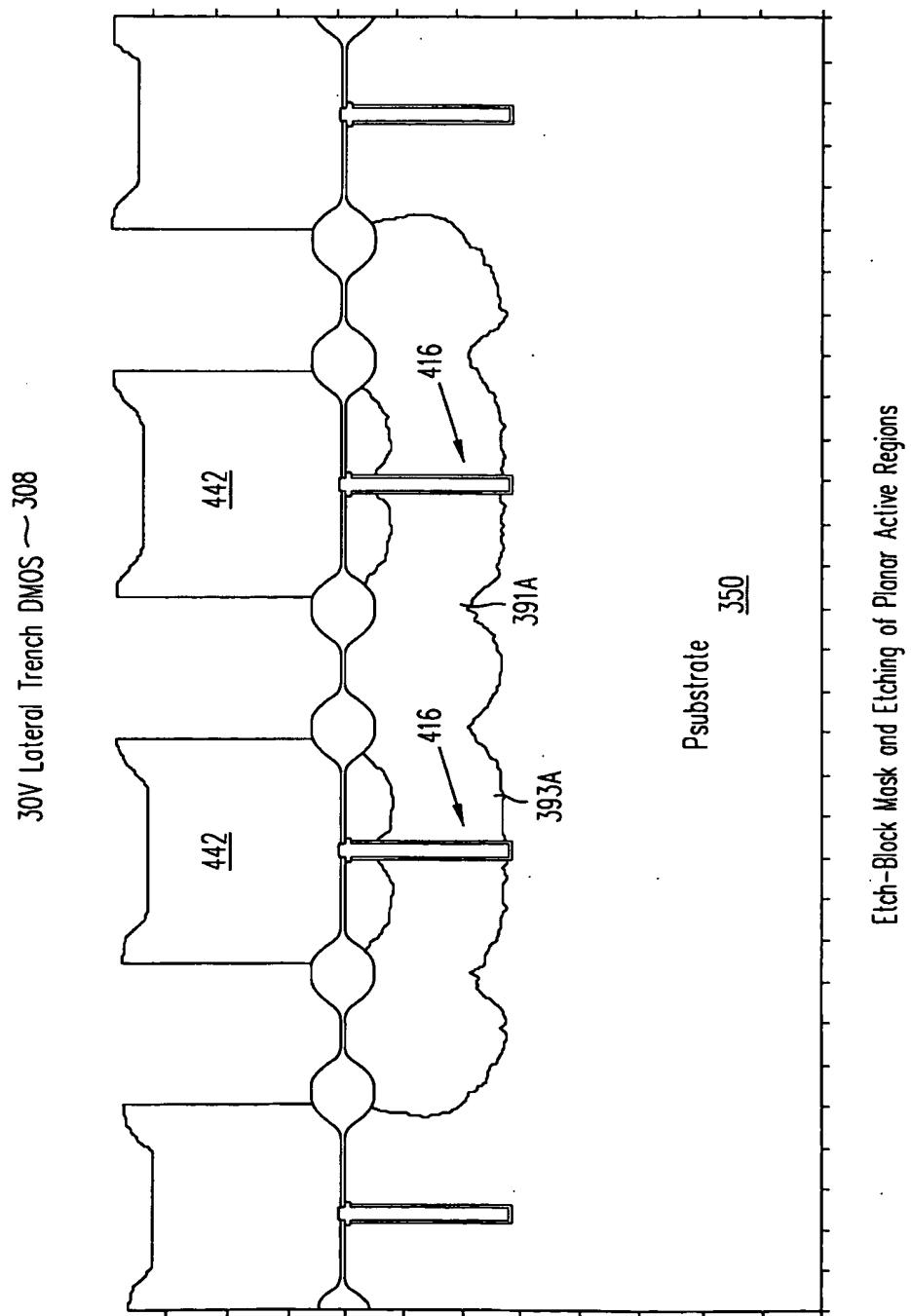
FIG. 46C

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5V P Well Implant-Second Stage

FIG. 46E



Etch-Block Mask and Etching of Planar Active Regions

FIG. 47D

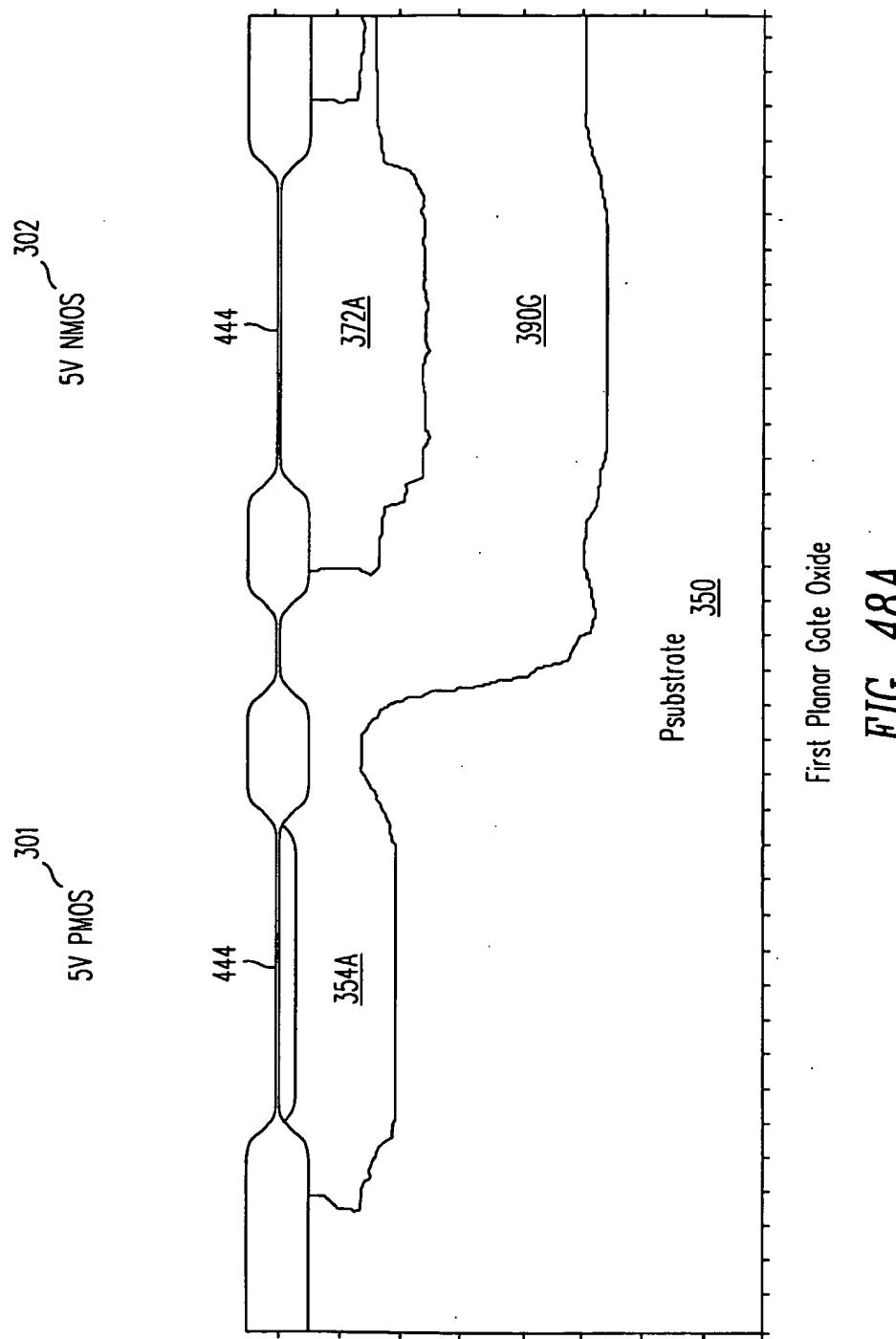
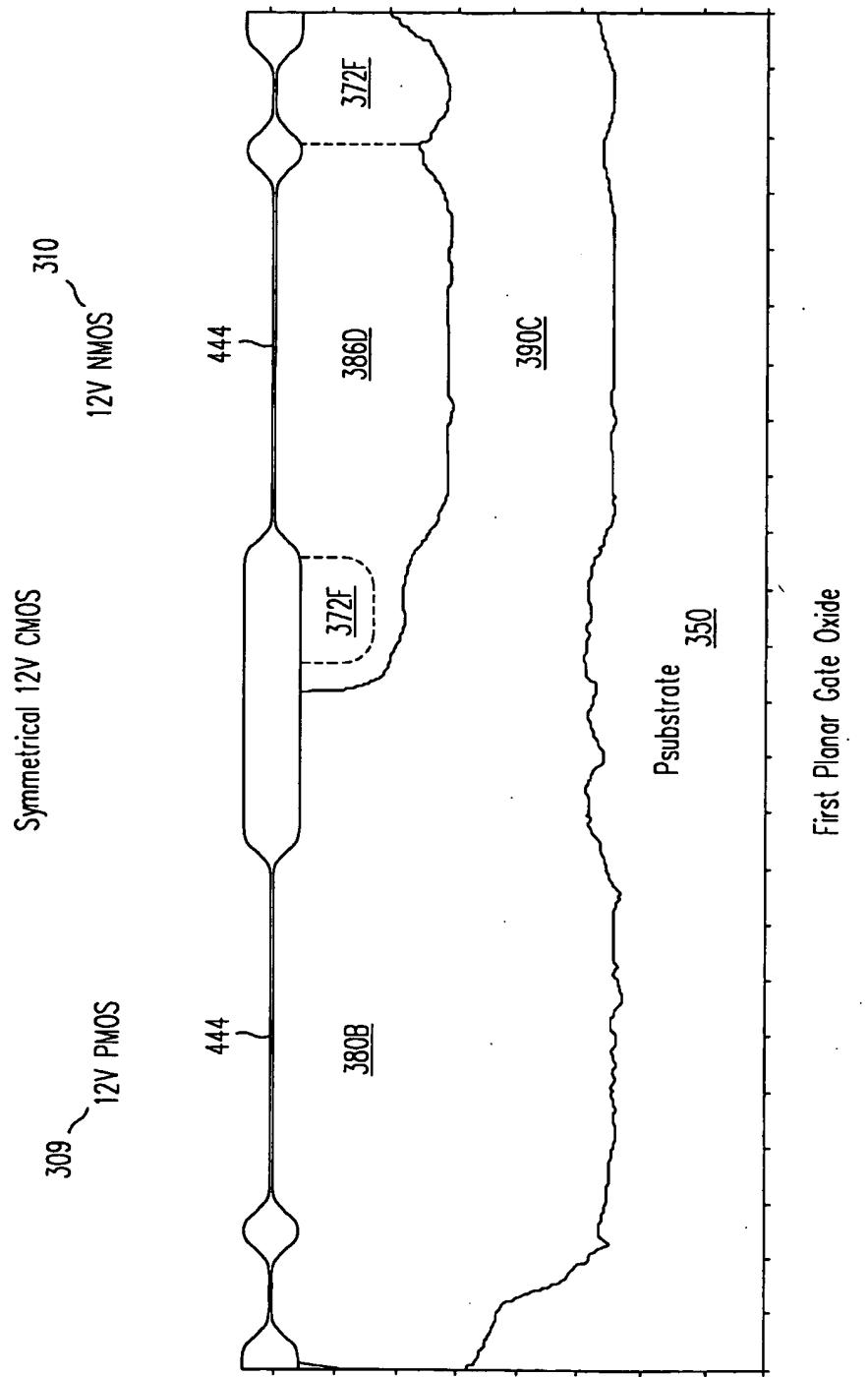
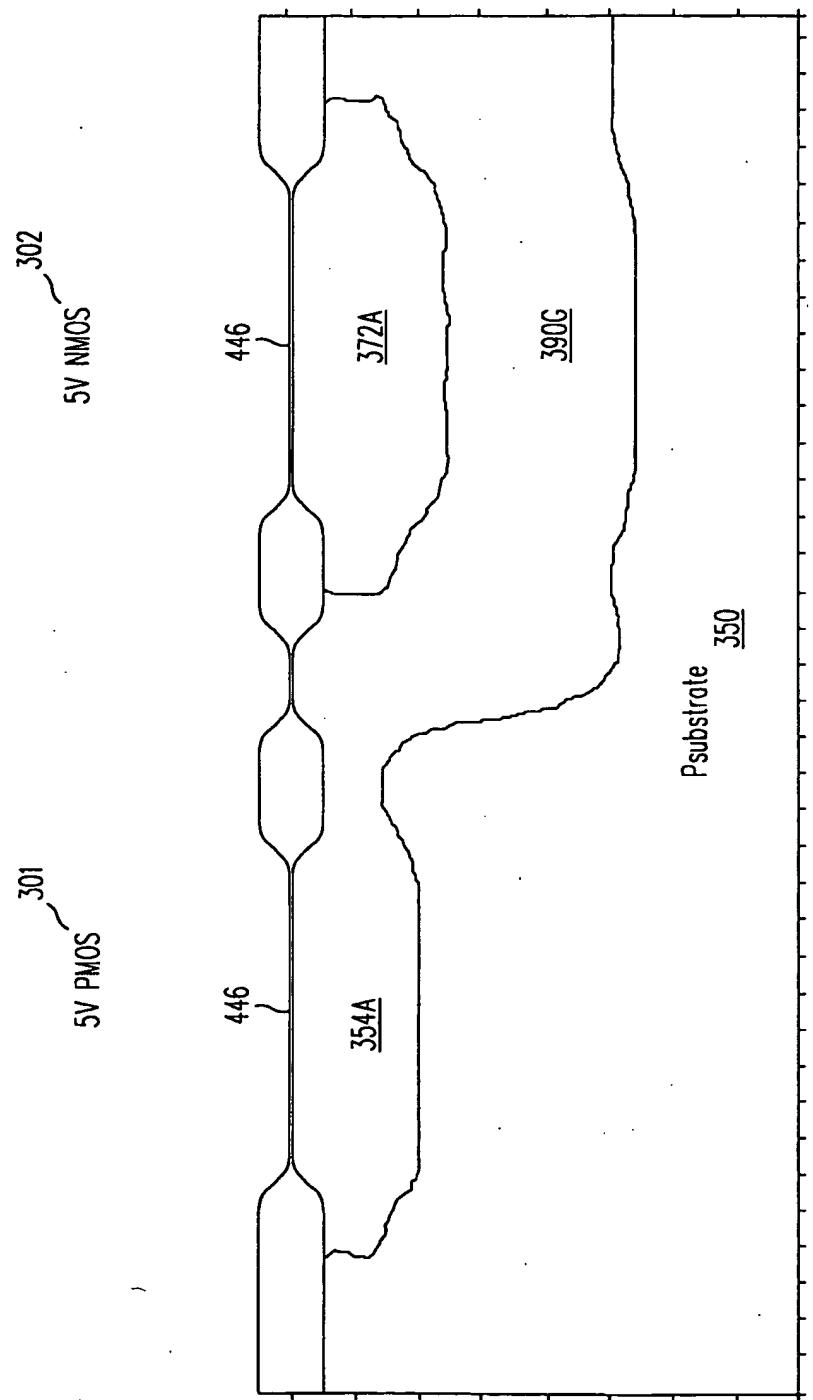


FIG. 48A

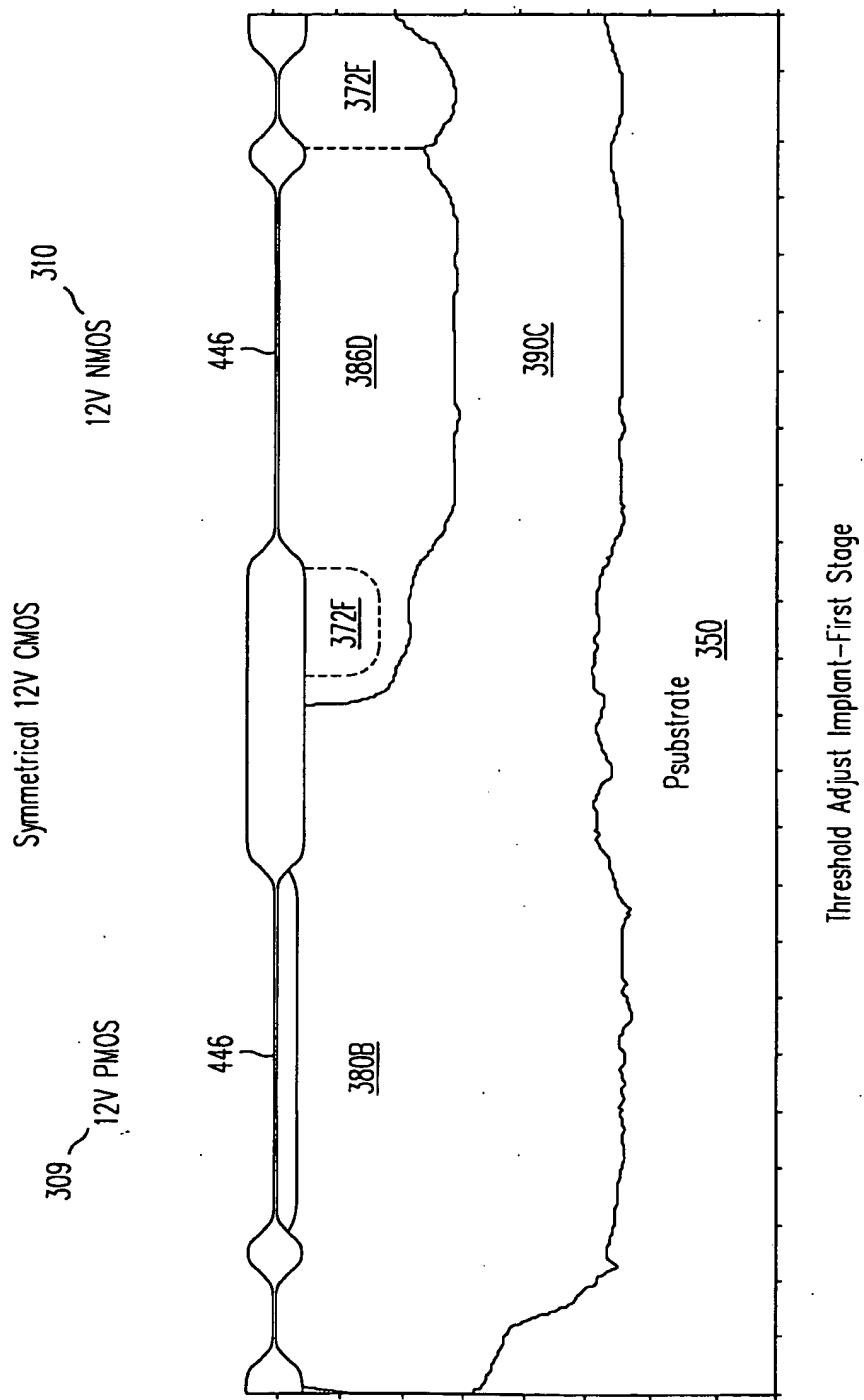


First Planar Gate Oxide
FIG. 48E



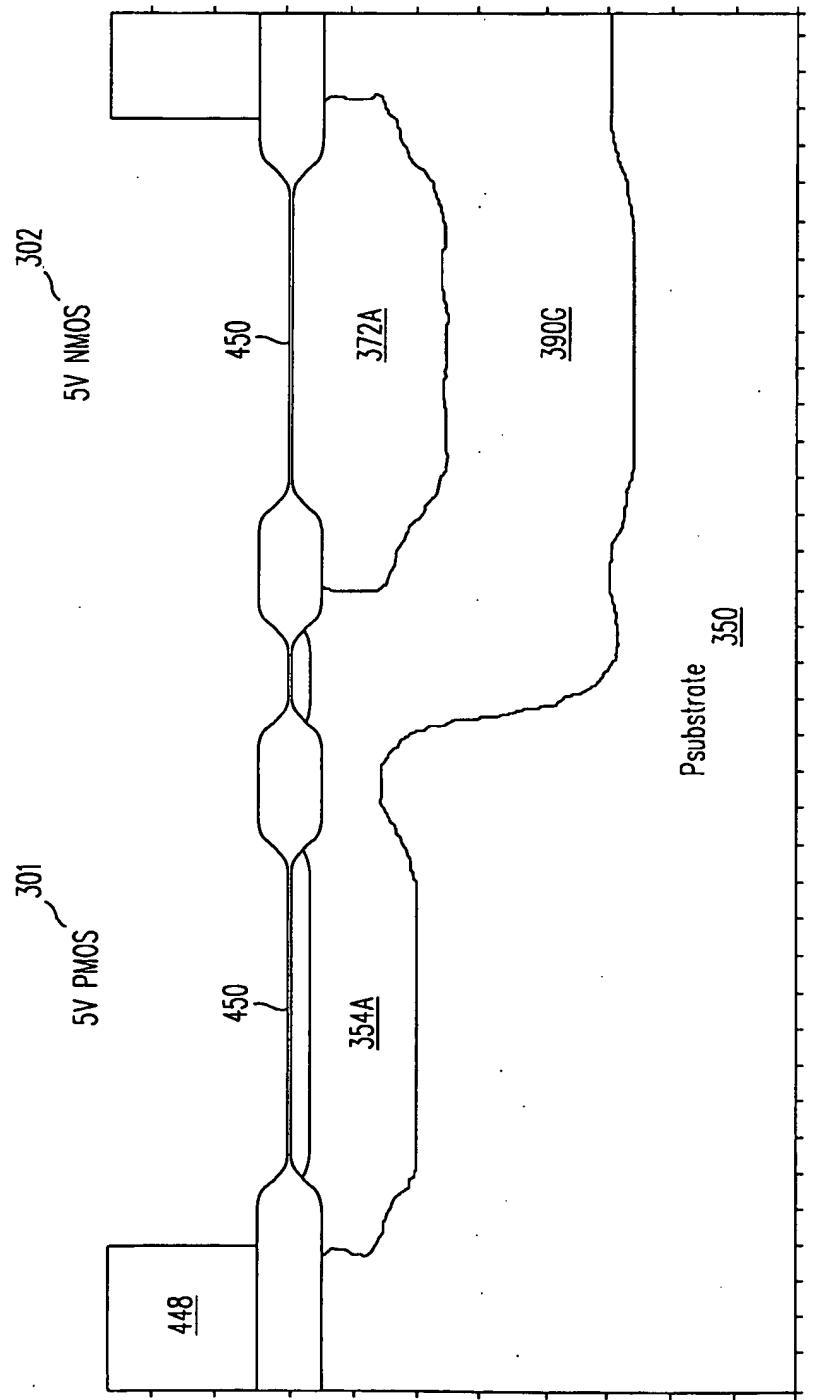
Threshold Adjust Implant-First Stage

FIG. 49A



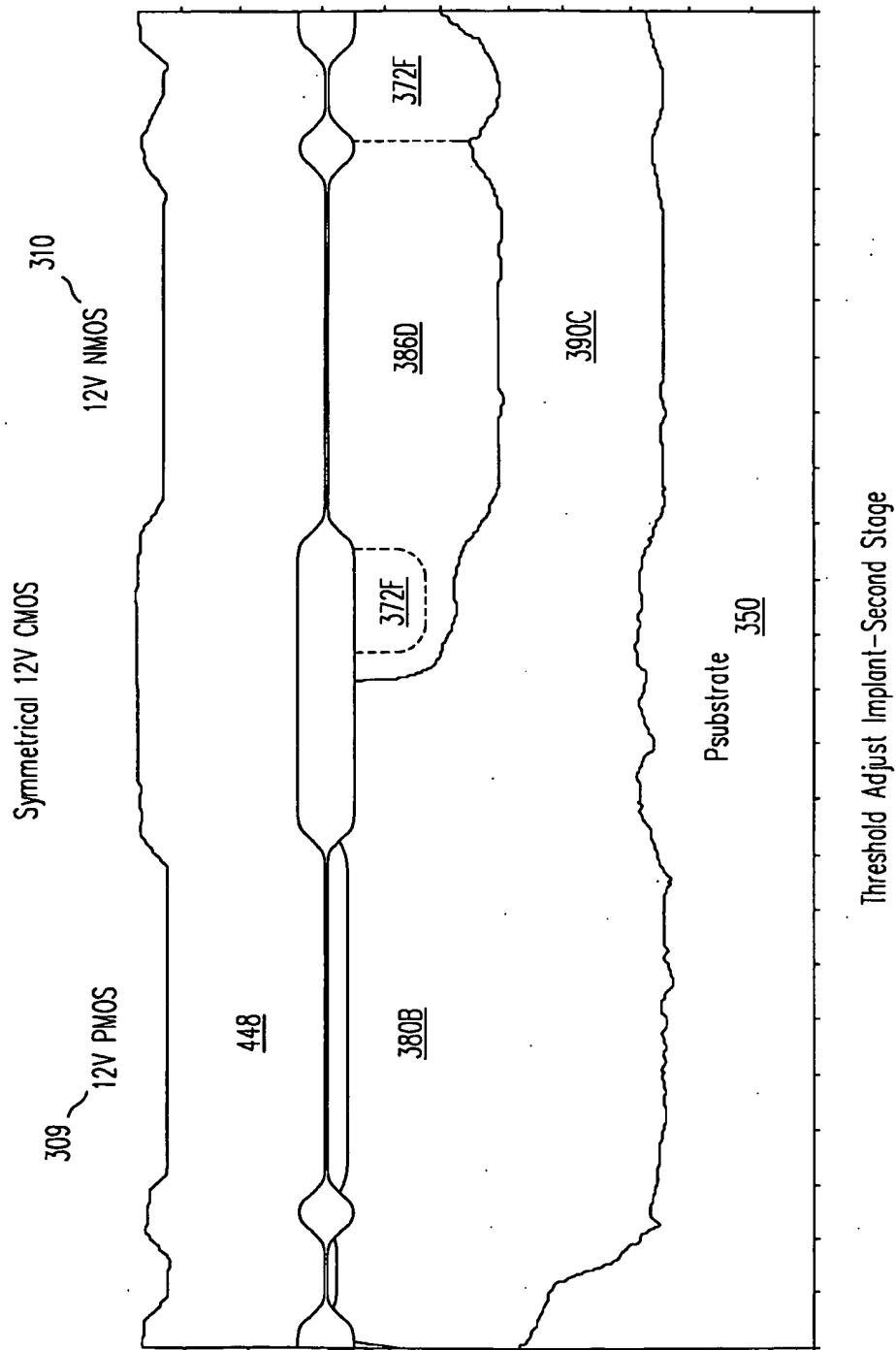
Threshold Adjust Implant-First Stage

FIG. 49E



Threshold Adjust Implant-Second Stage
First Planar Gate Oxide Removal

FIG. 50A



Threshold Adjust Implant-Second Stage

FIG. 50E

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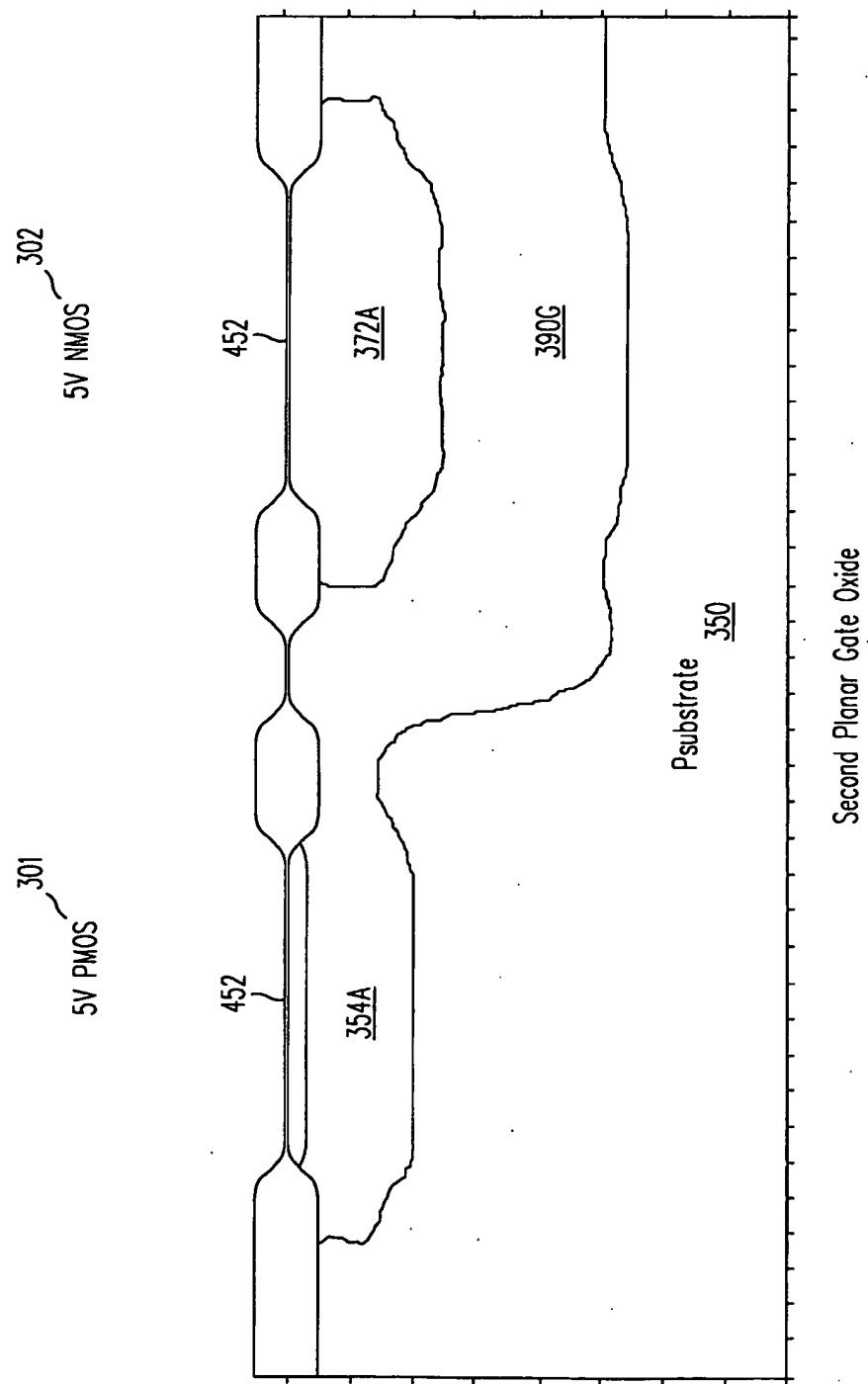
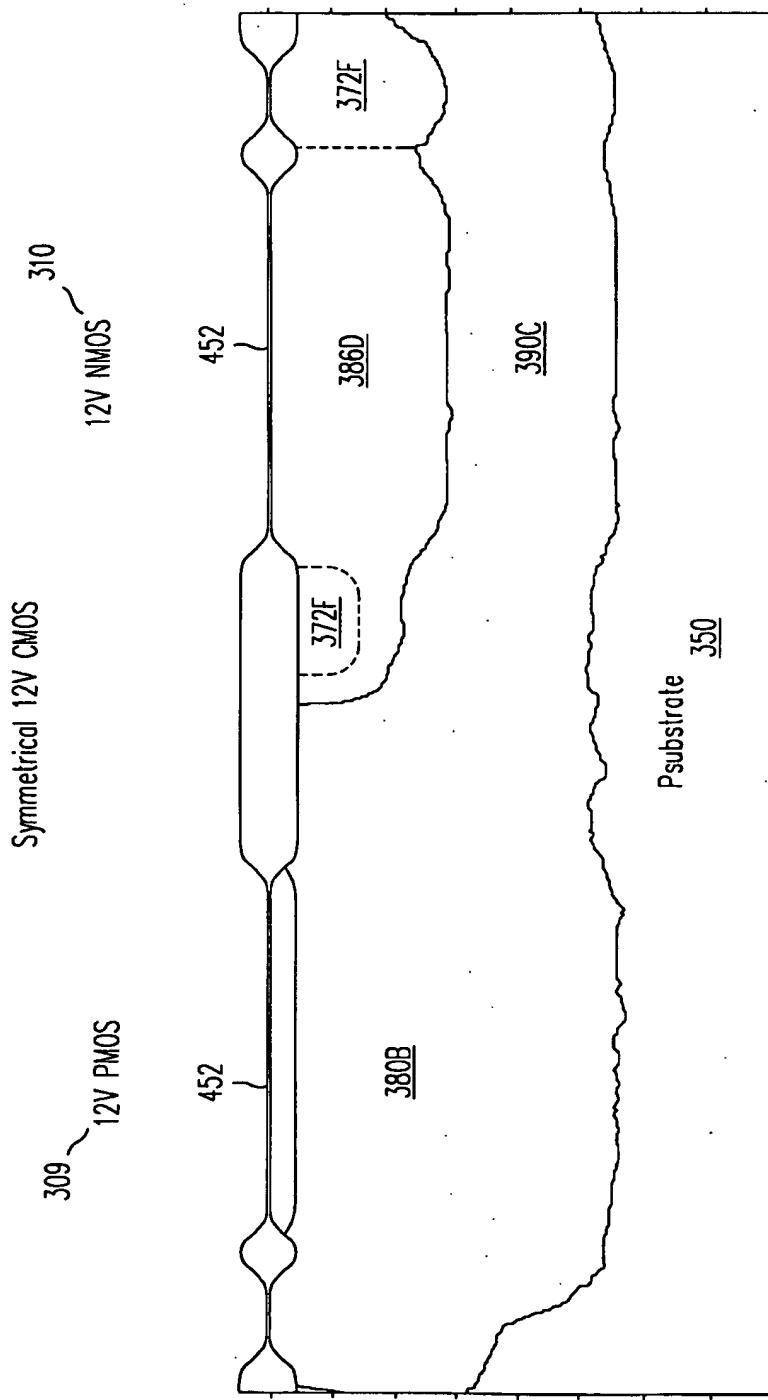


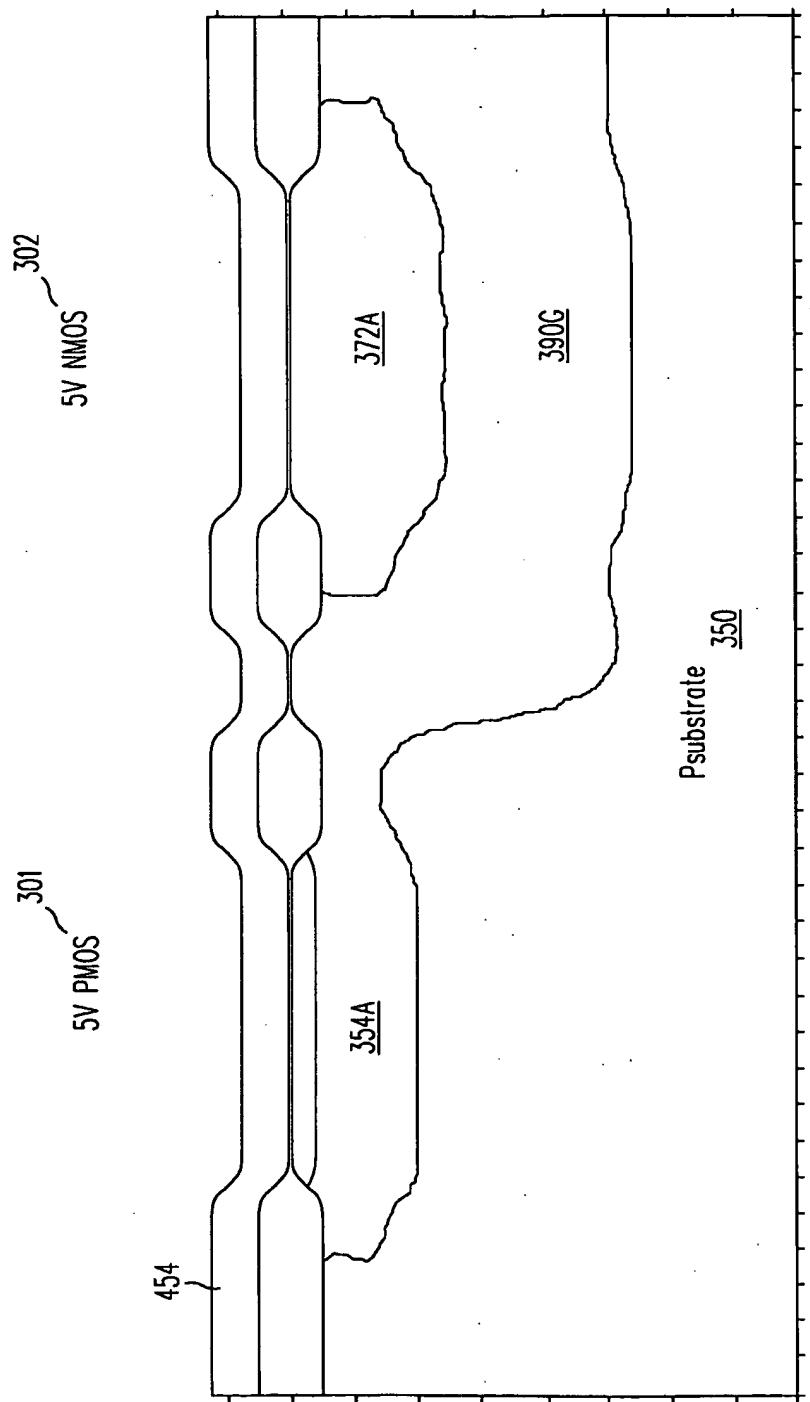
FIG. 51A



Second Planar Gate Oxide

FIG. 51E

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Polysilicon-Third Layer

FIG. 52A

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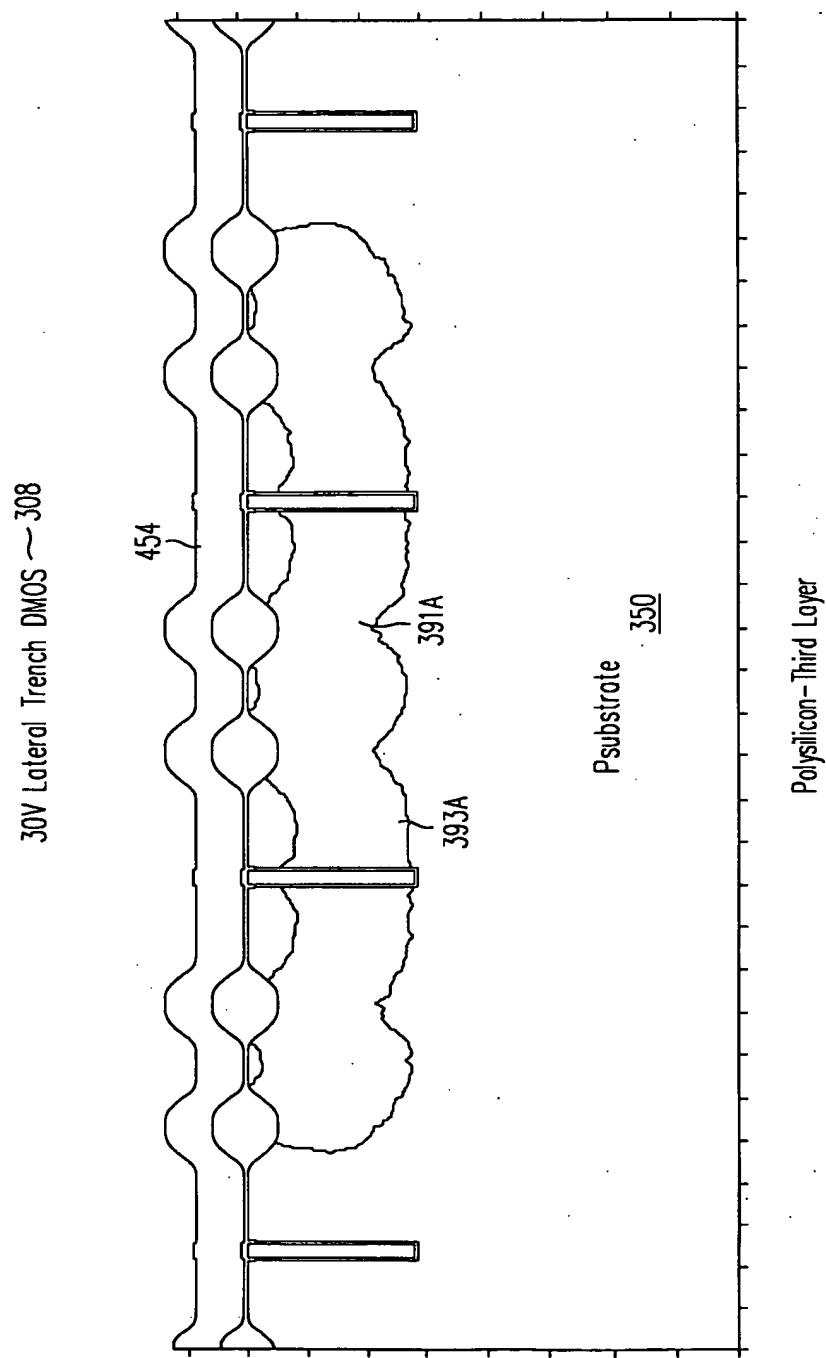


FIG. 52D

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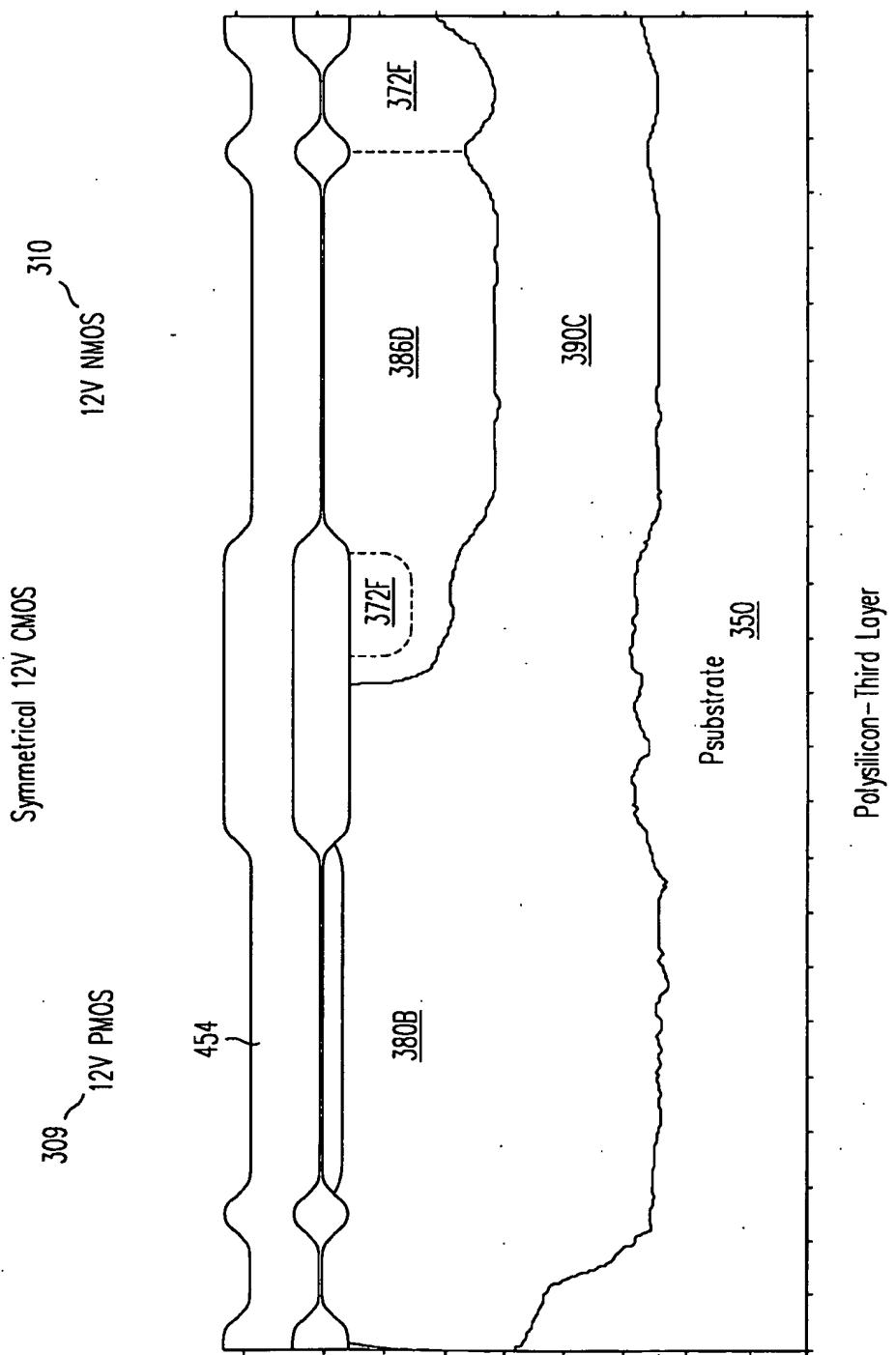
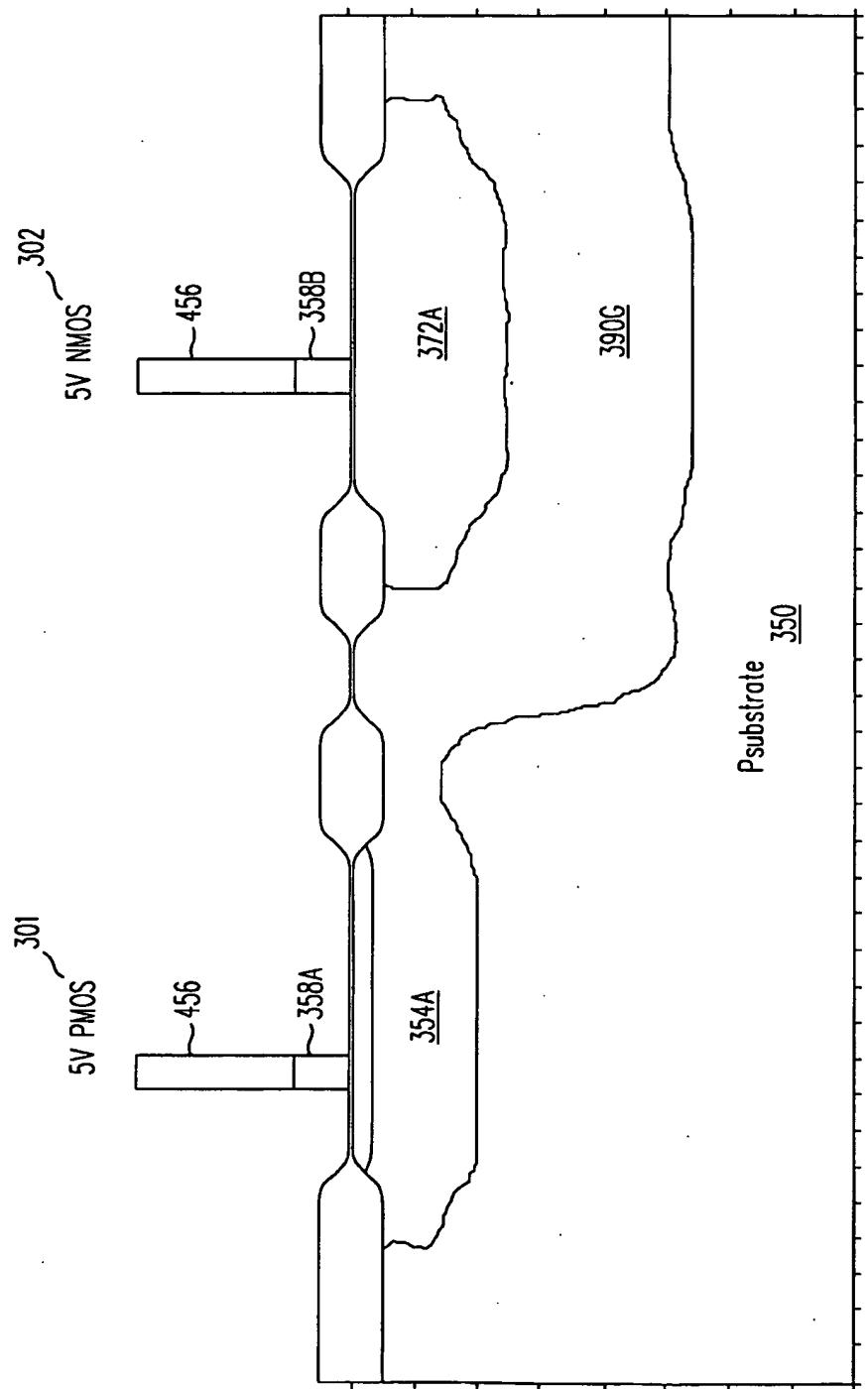
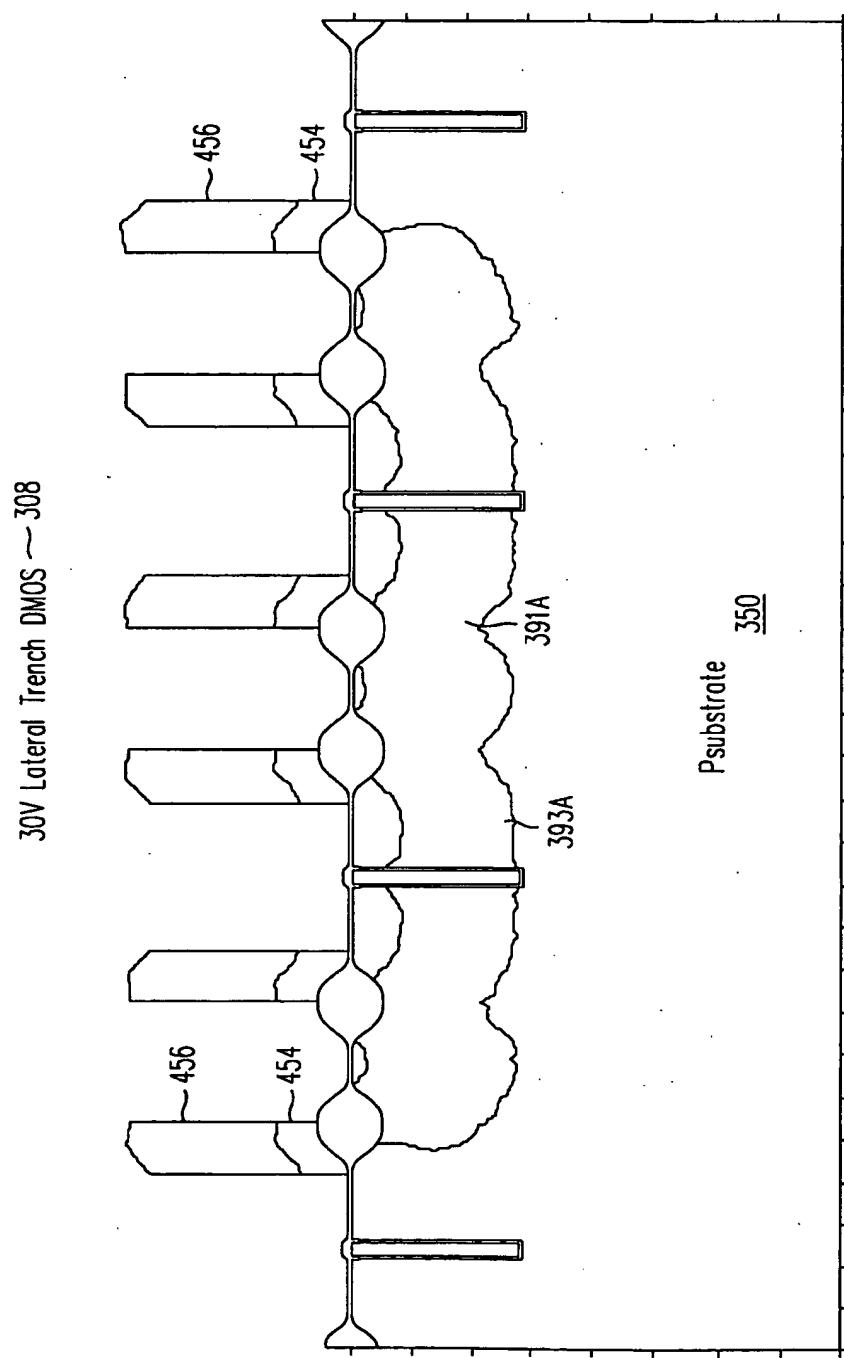


FIG. 52E



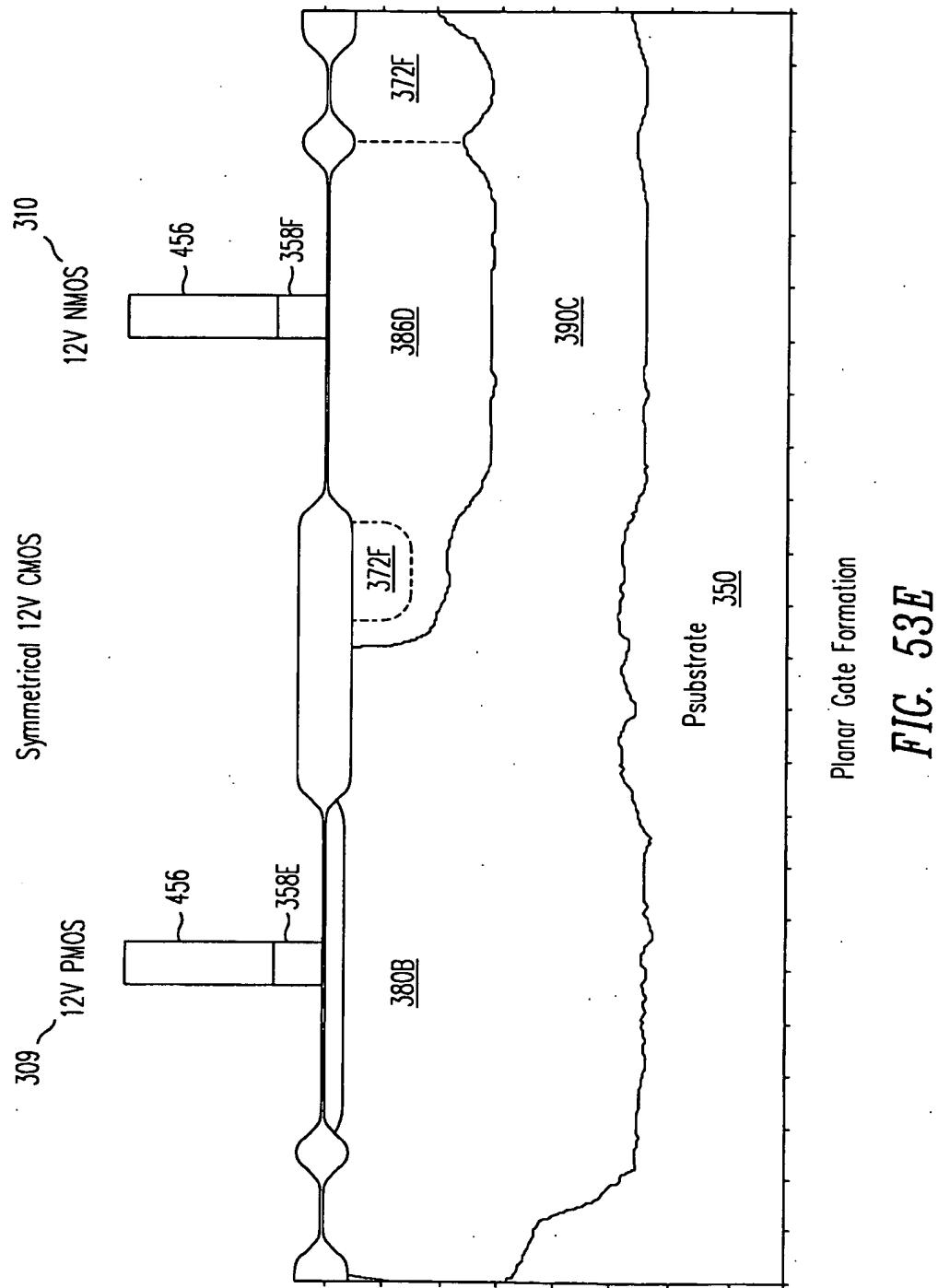
Planar Gate Formation

FIG. 53A



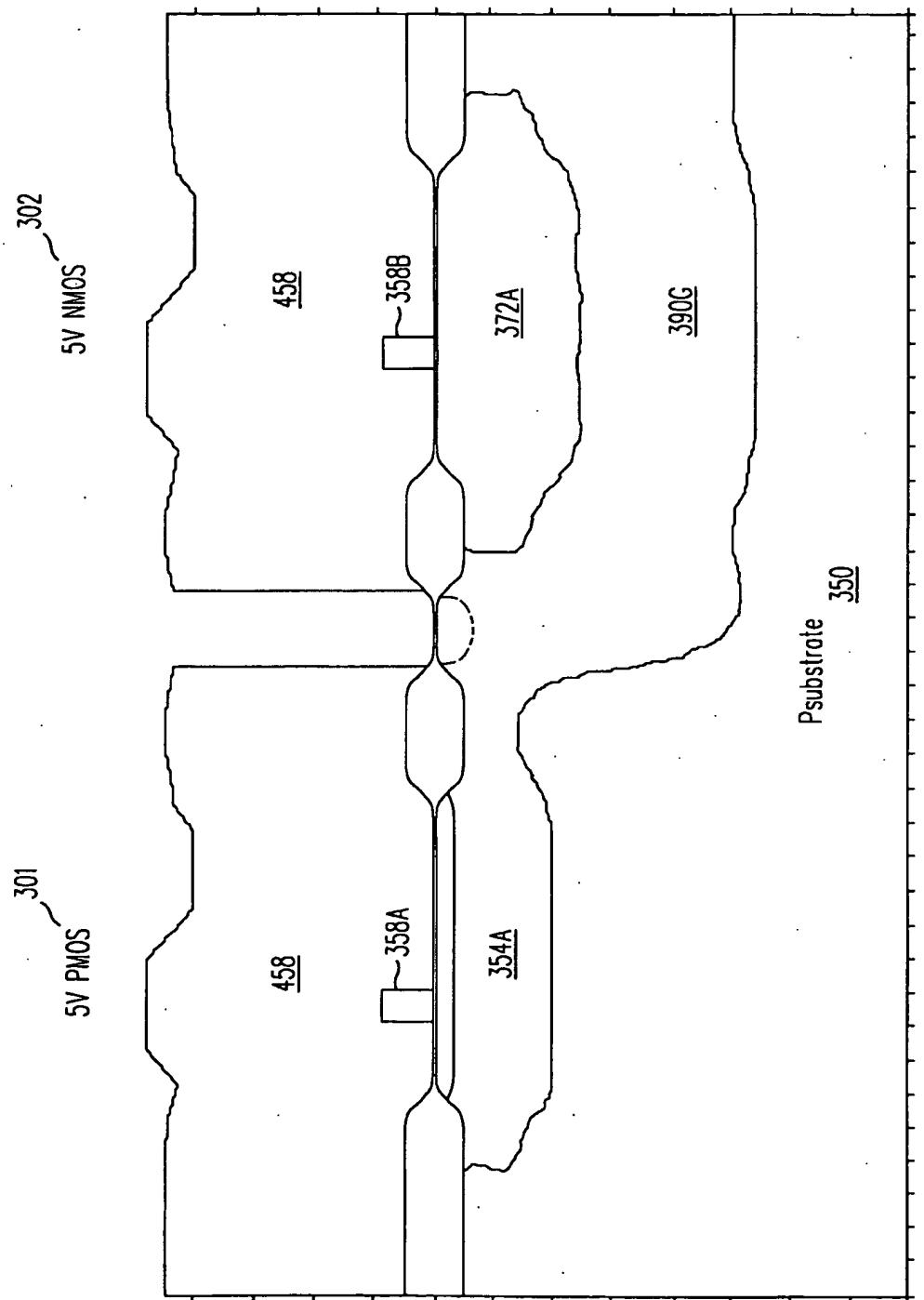
Planar Gate Formation

FIG. 53D



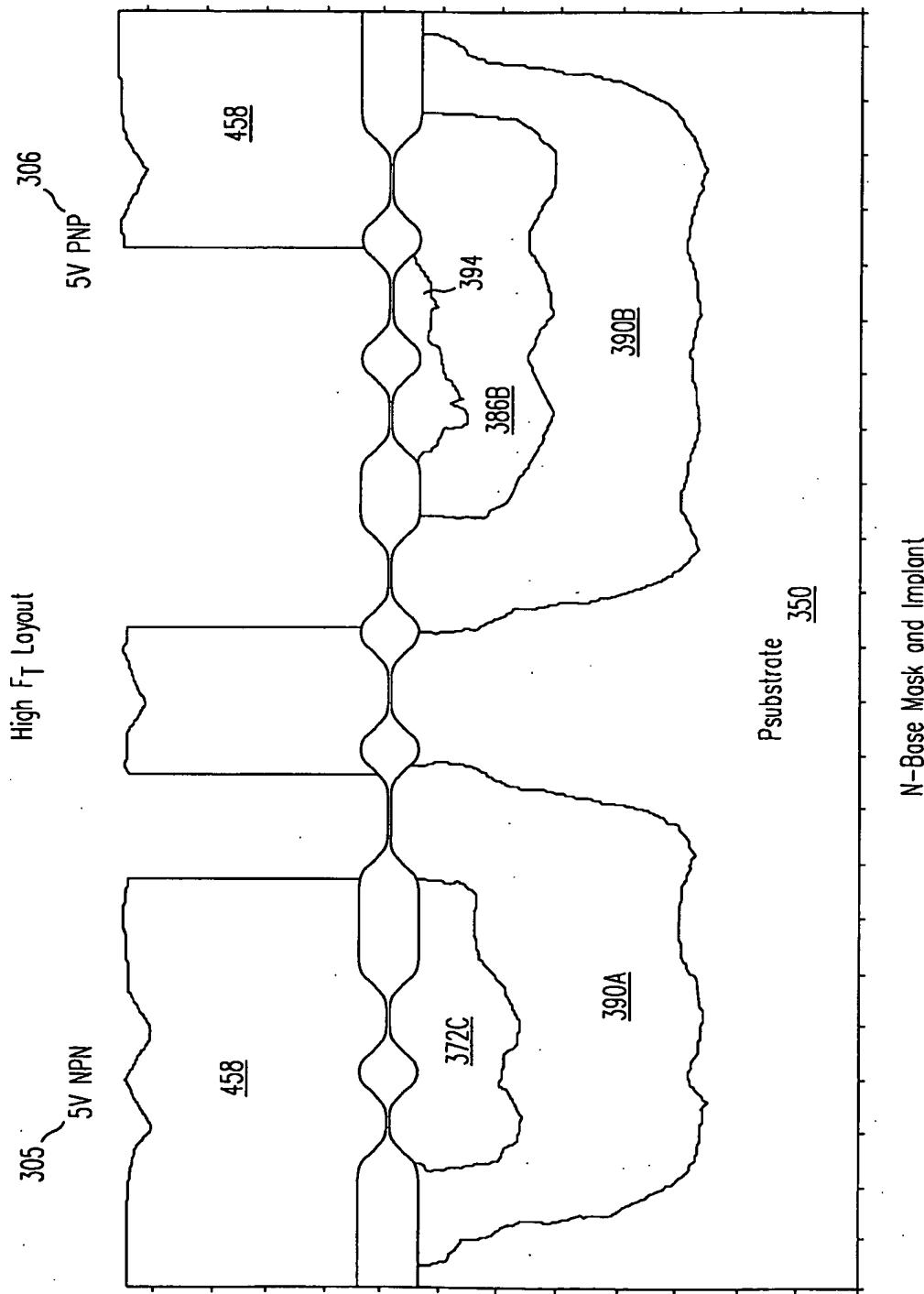
Planar Gate Formation

FIG. 53E



N-Base Mask and Implant

FIG. 54A



N-Base Mask and Implant

FIG. 54B

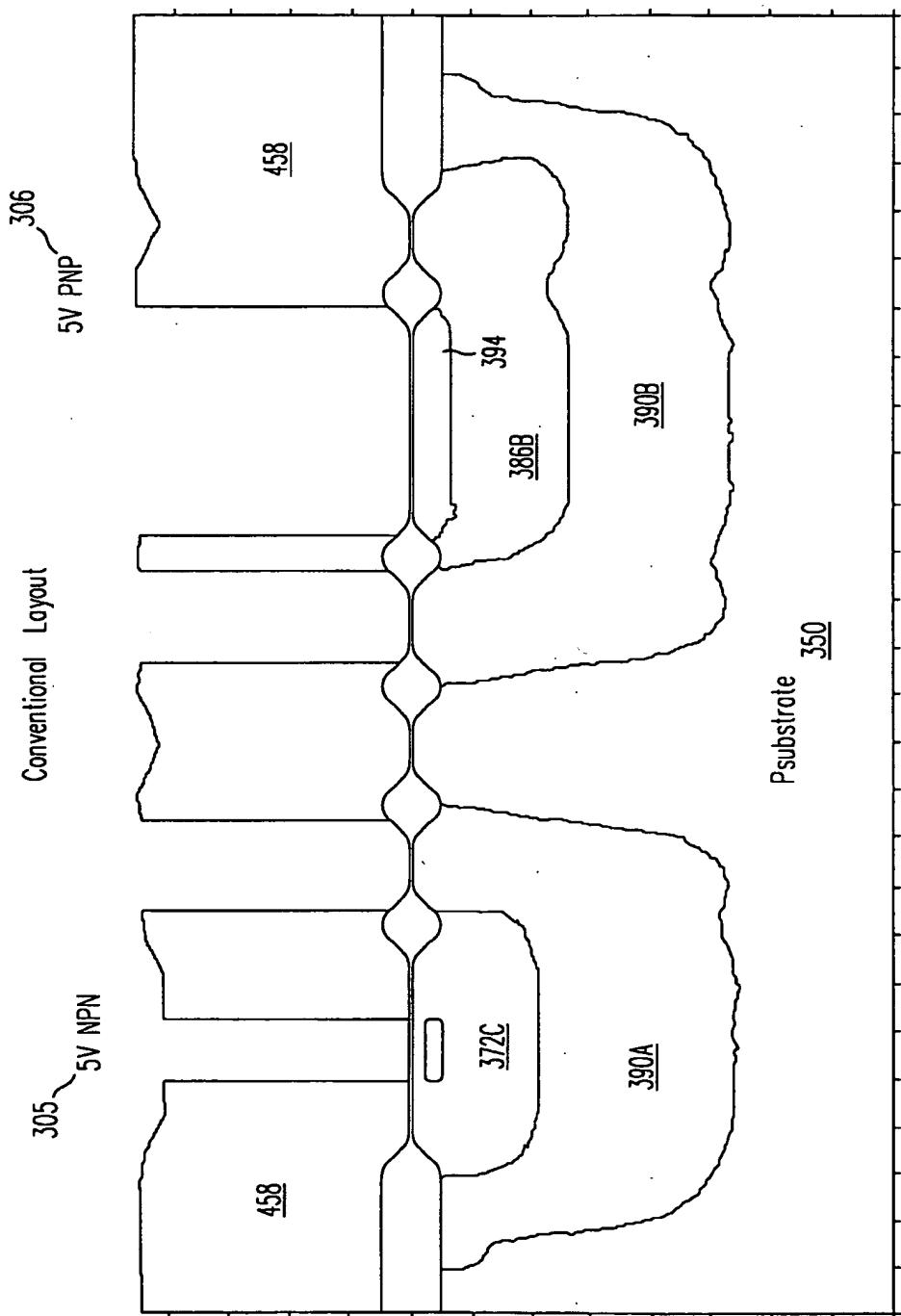


FIG. 54C

N-Base Mask and Implant

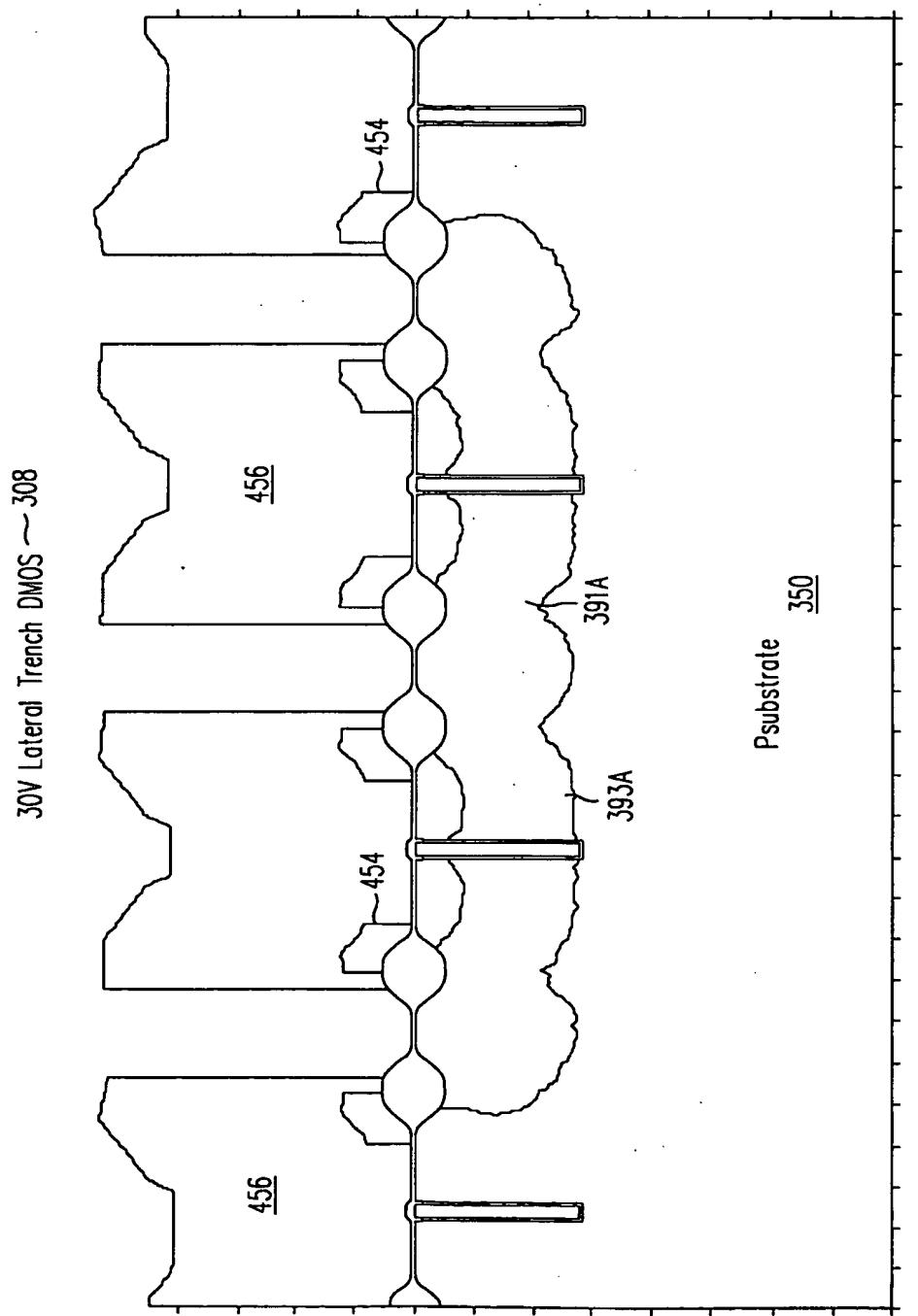
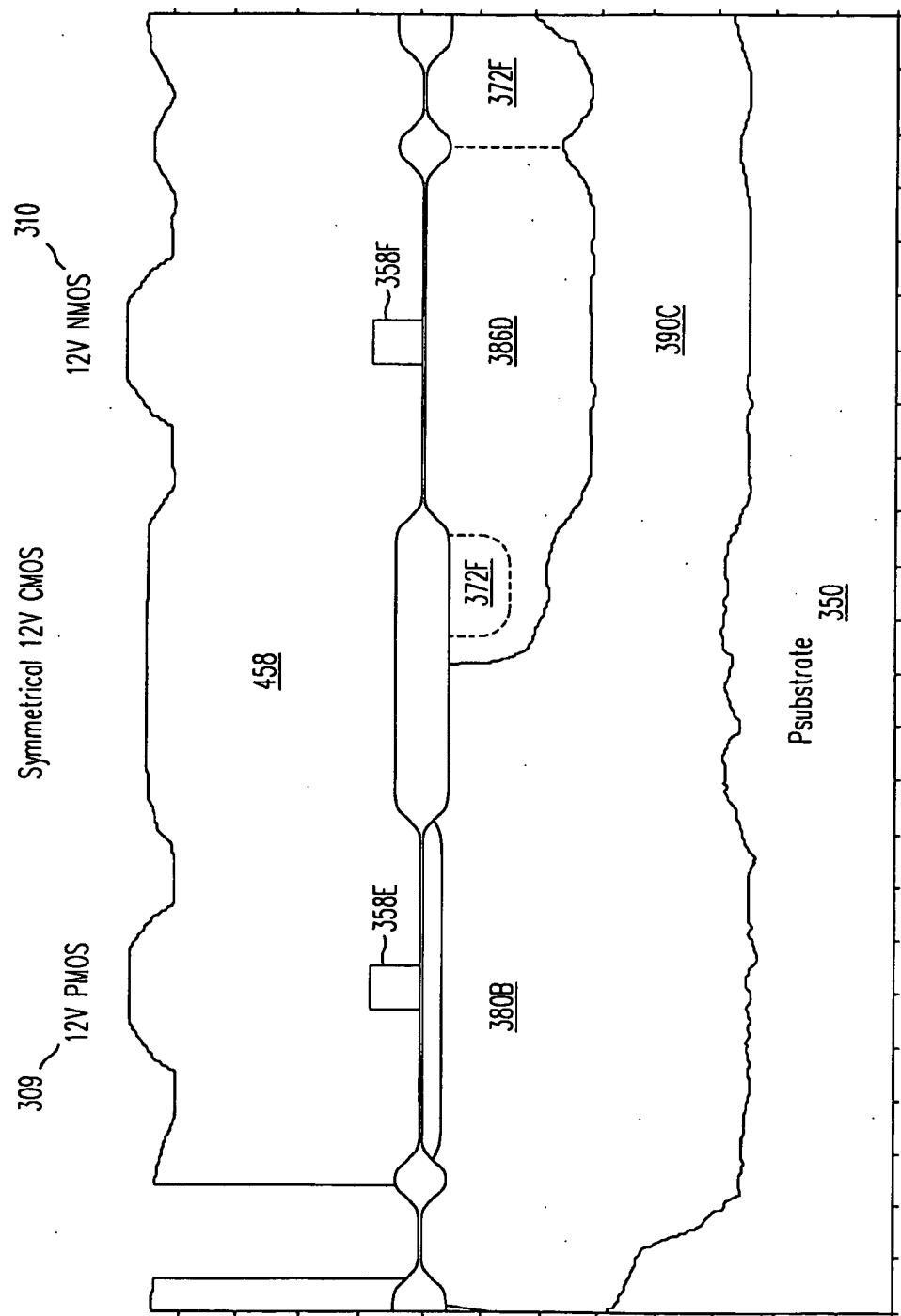


FIG. 54D

N-Base Mask and Implant

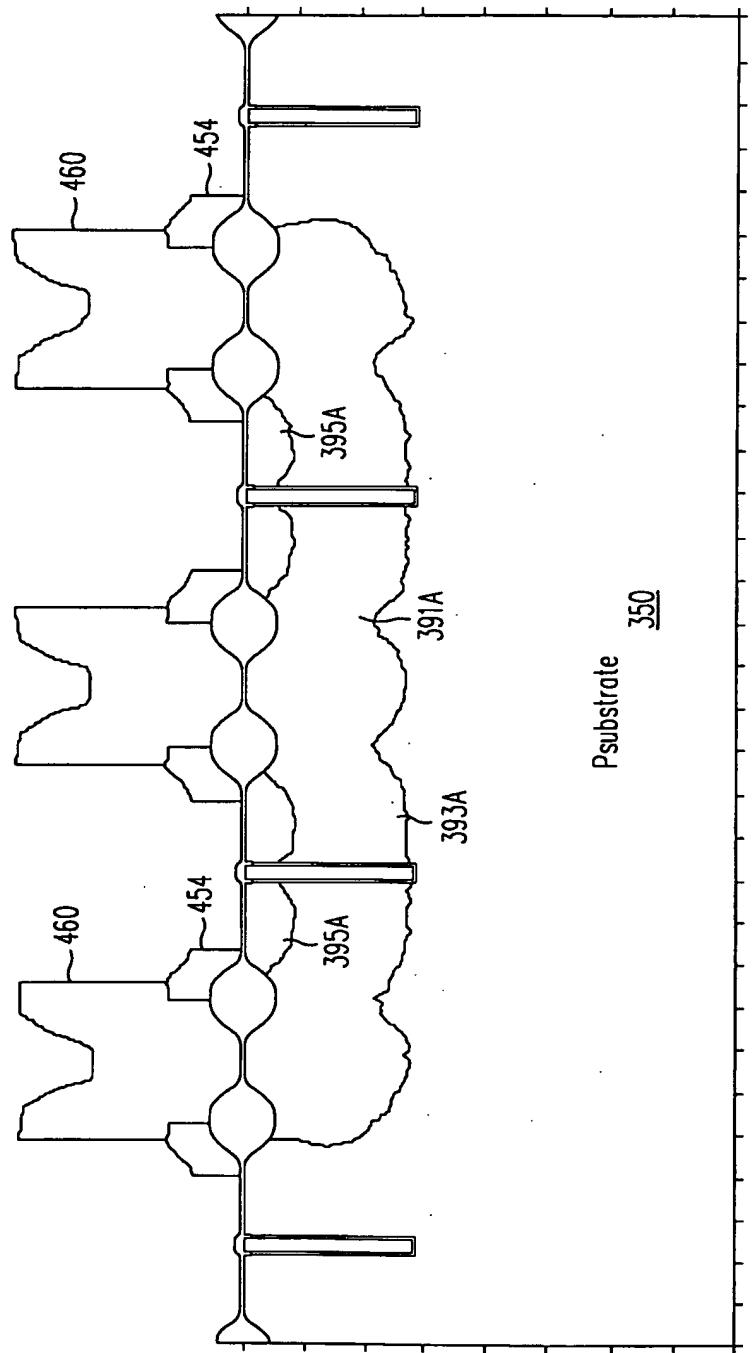
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N-Base Mask and Implant

FIG. 54E

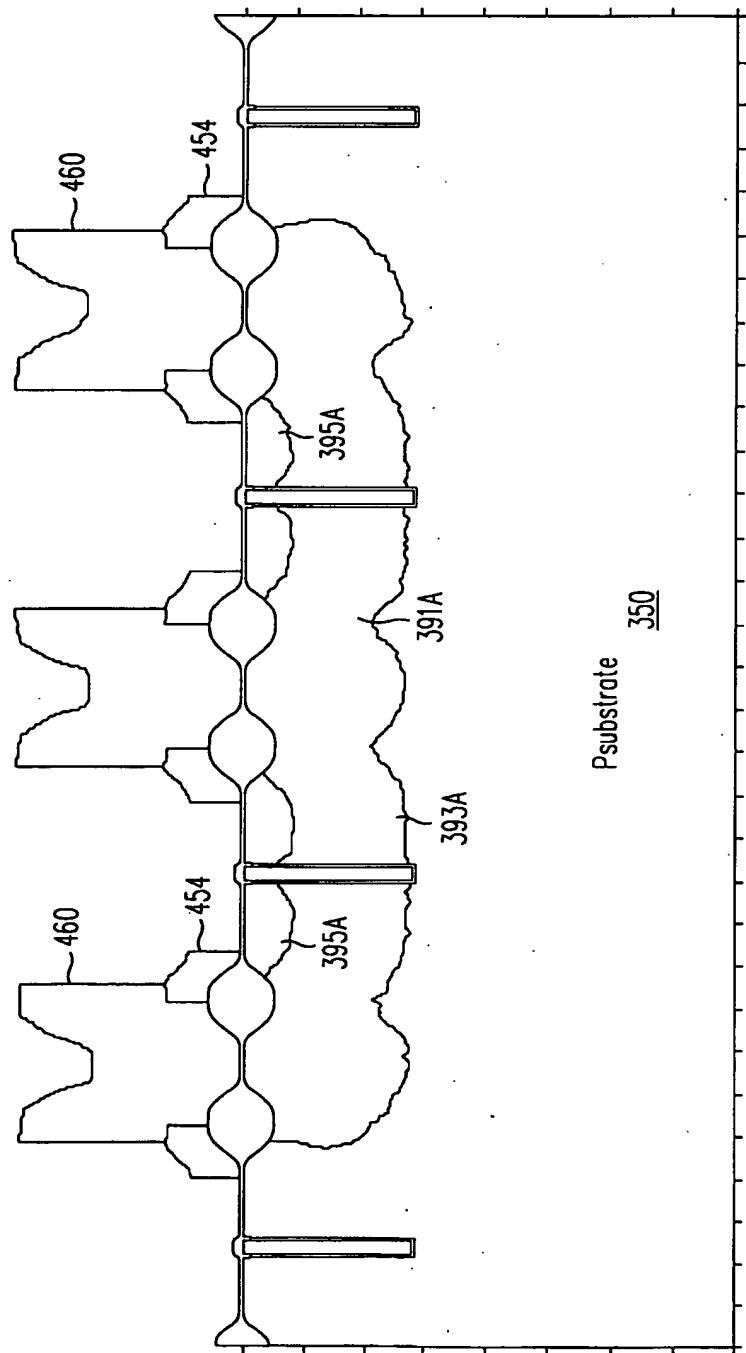
30V Lateral Trench DMOS ~ 308



P Body Mask and Implant-First Stage

FIG. 55D

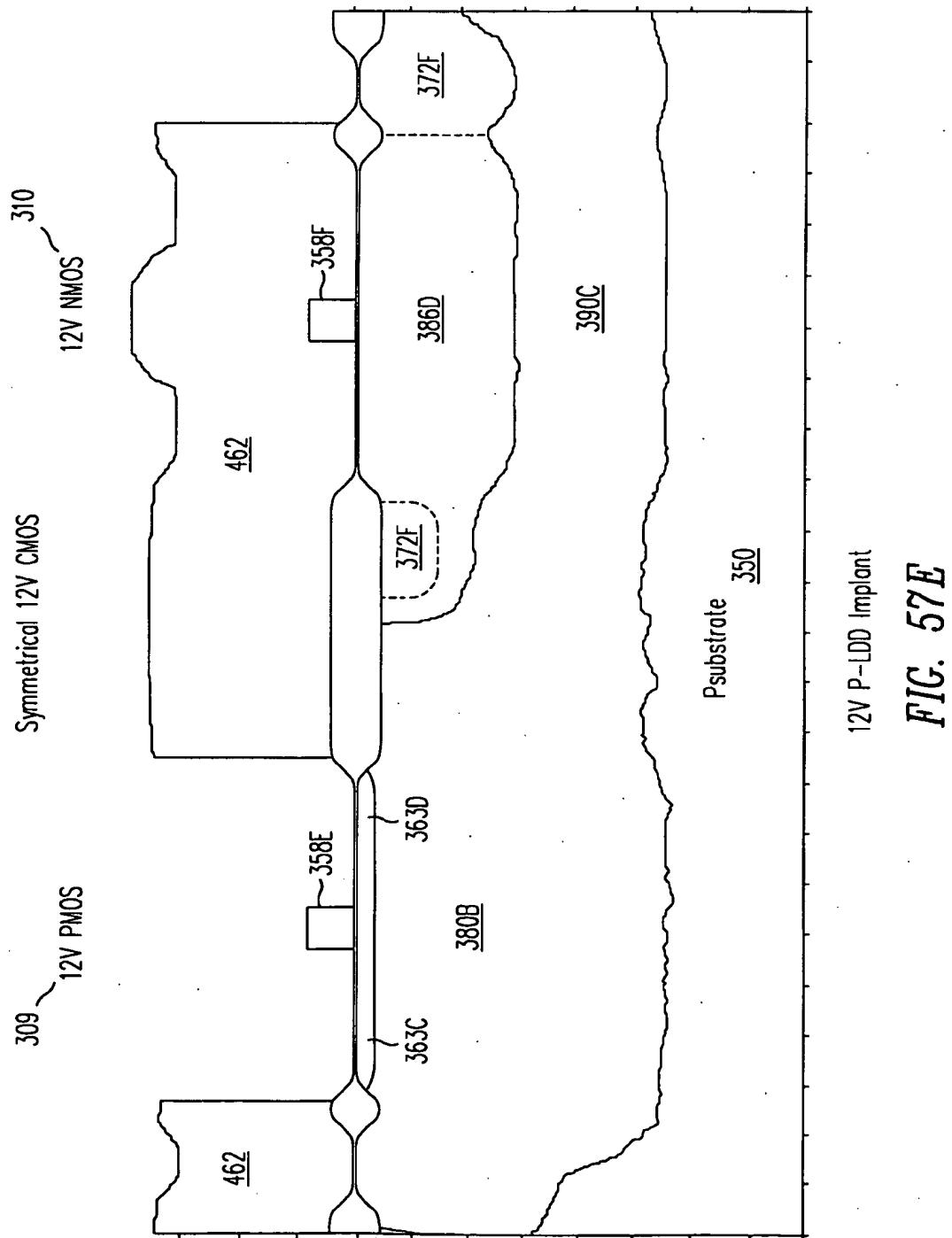
30V Lateral French DMOS — 308



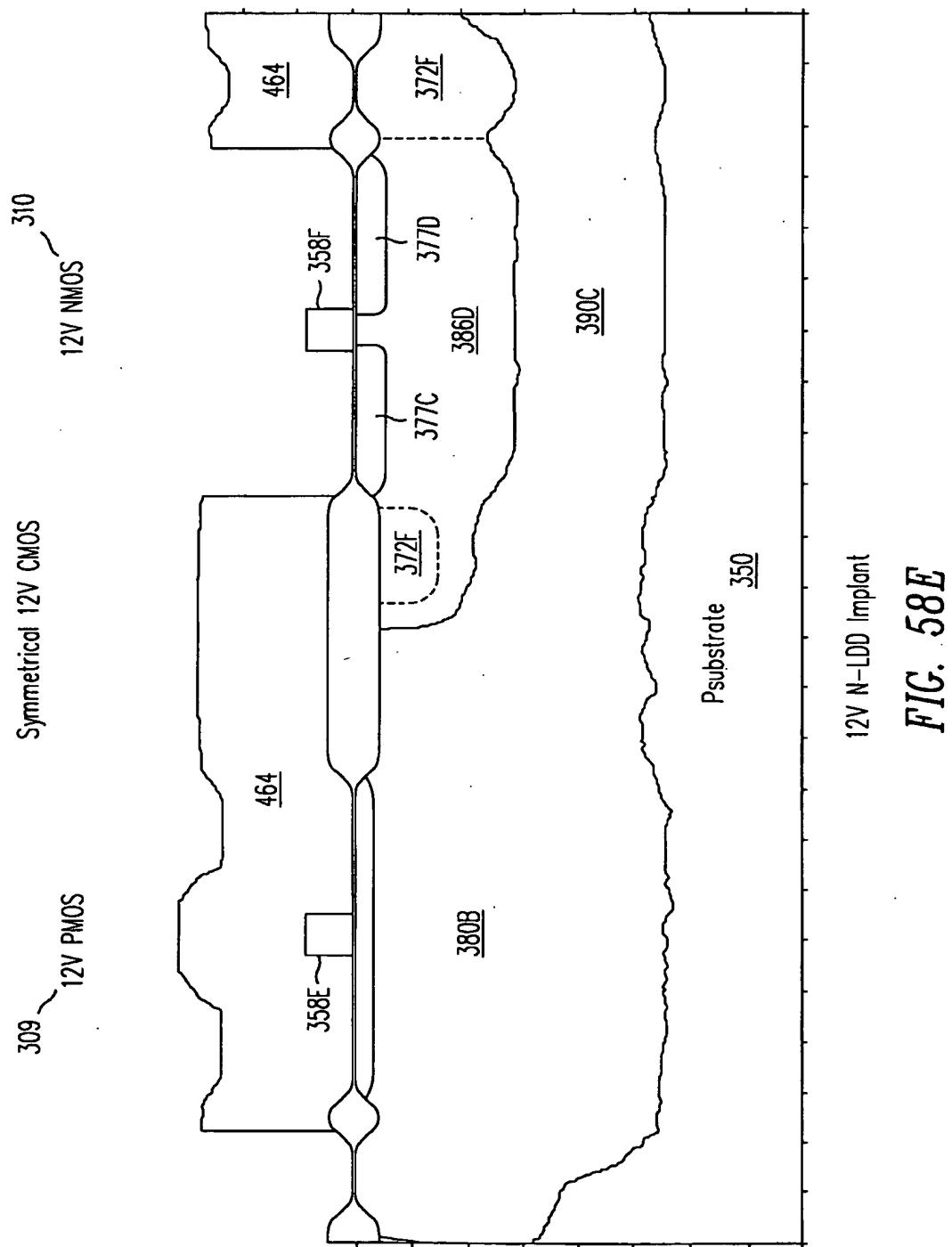
P Body Mask and Implant—Second Stage

FIG. 56D

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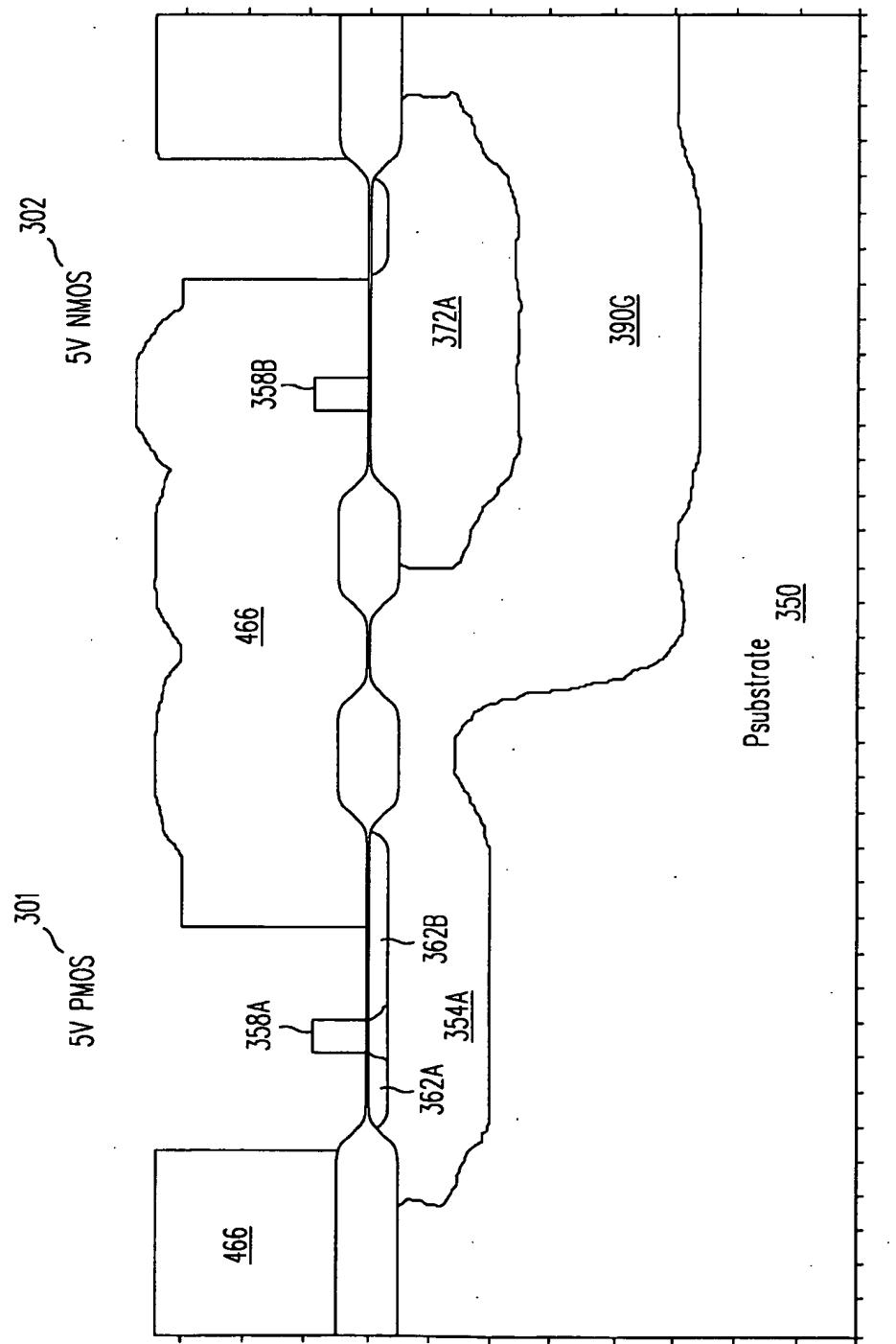
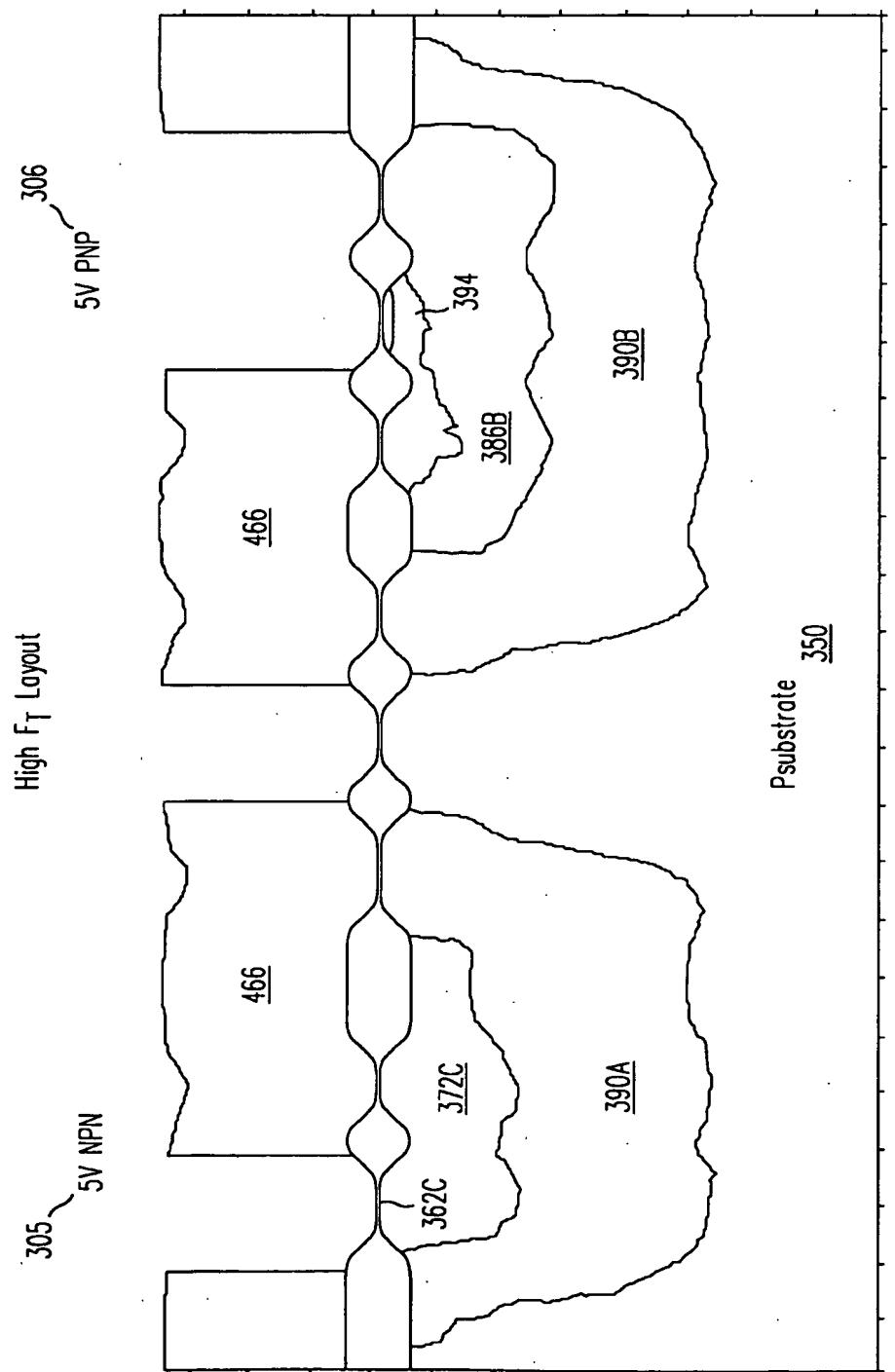


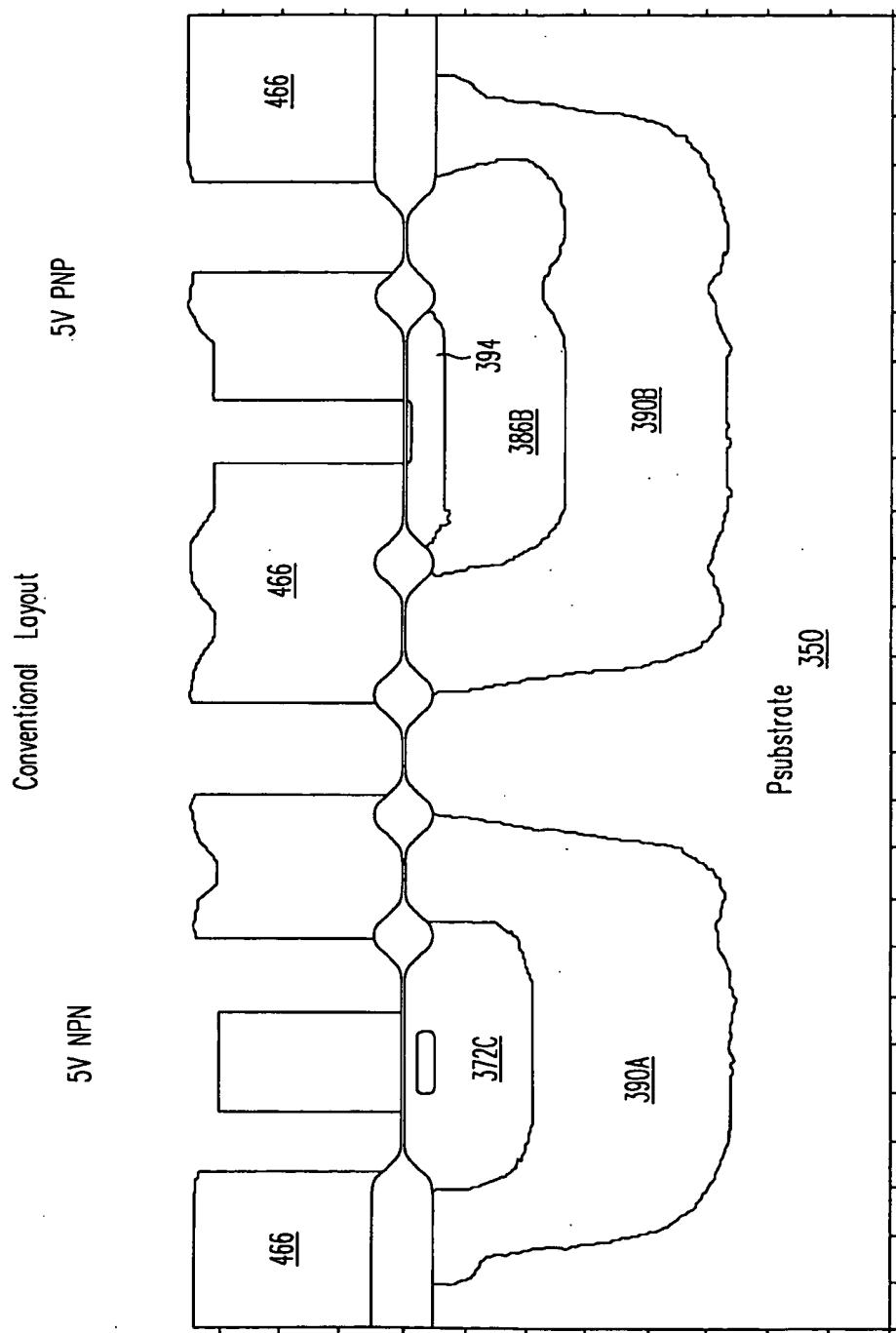
FIG. 59A

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5V P-LDD Implant

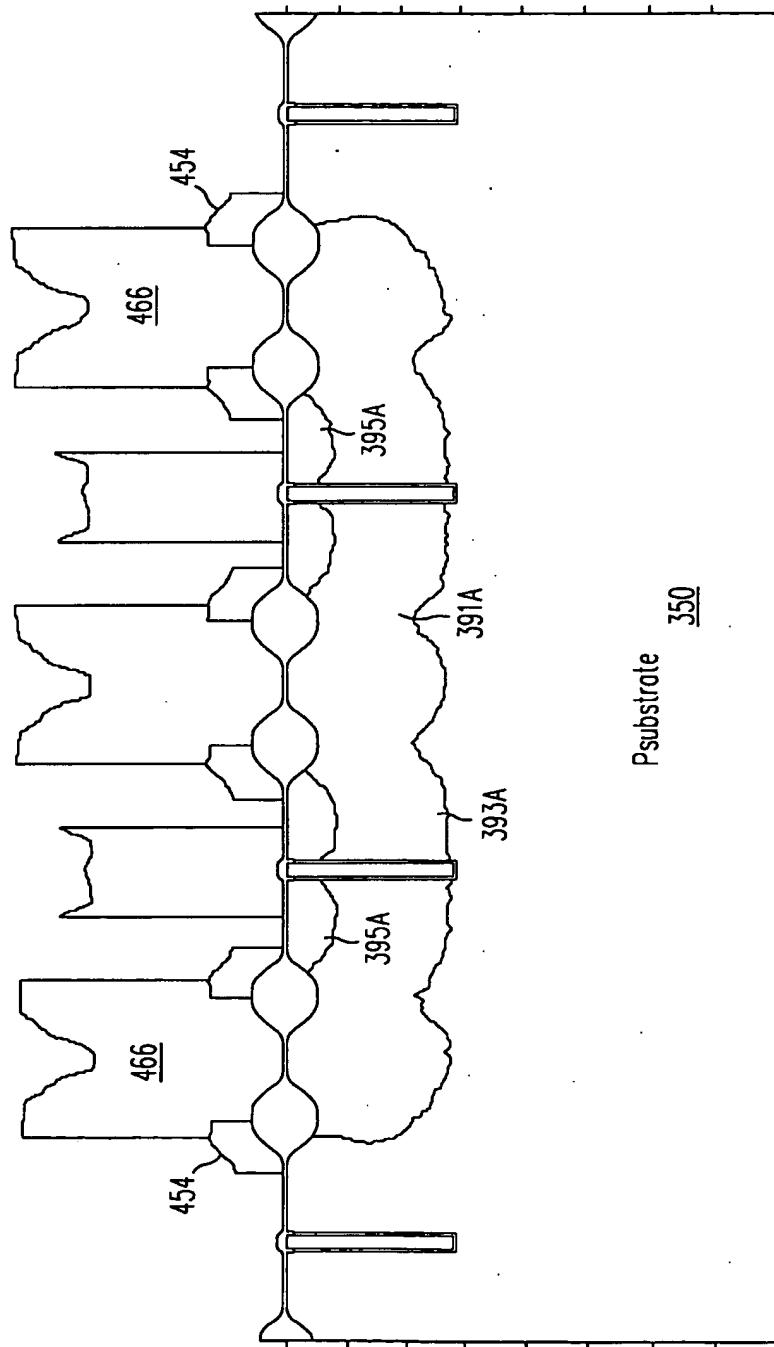
FIG. 59B



5V P-LDD Implant

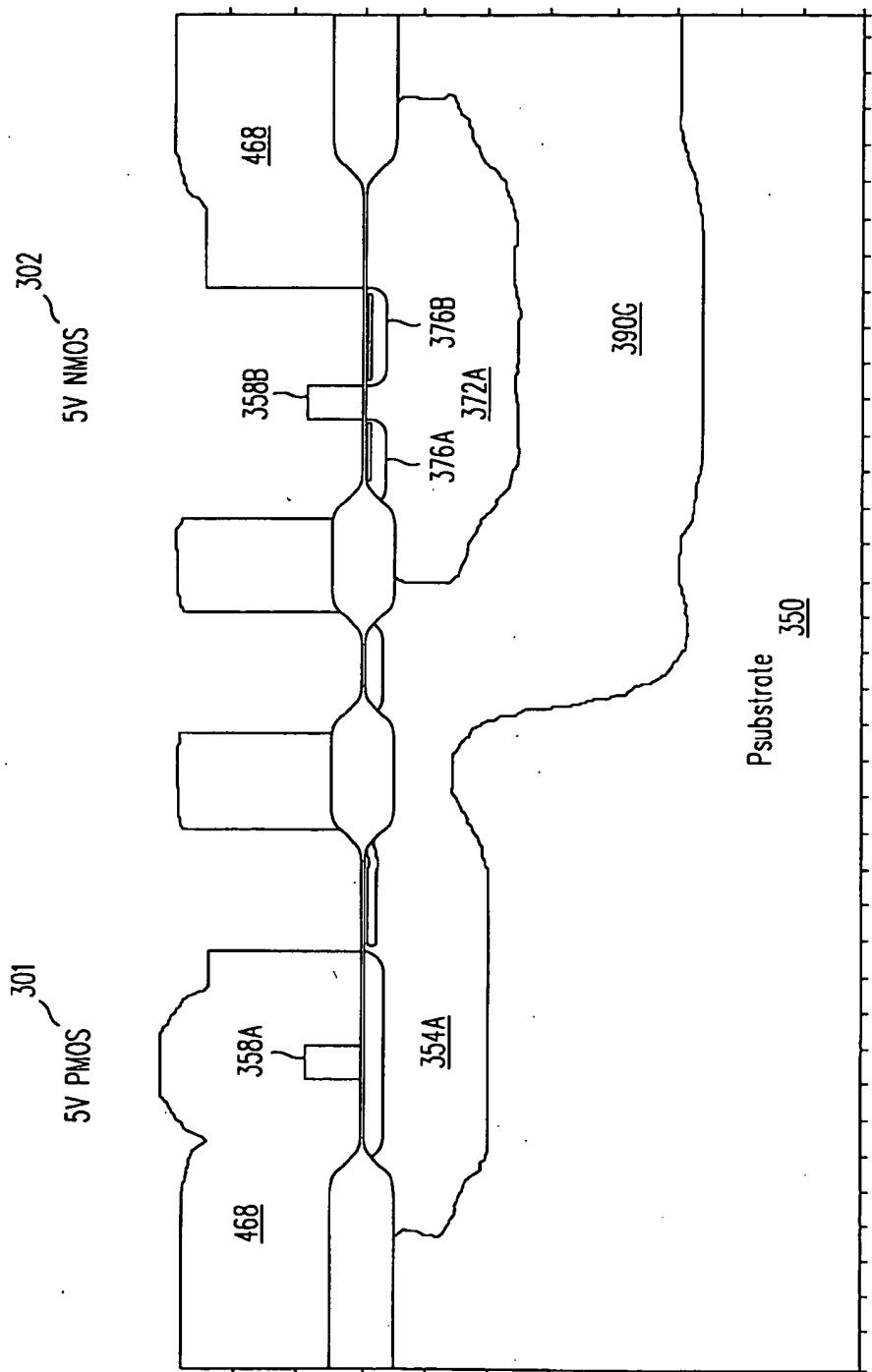
FIG. 59C

30V Lateral trench DMOS — 308



5V P-LDD implant

FIG. 59D



5V N-LDD implant

FIG. 60A

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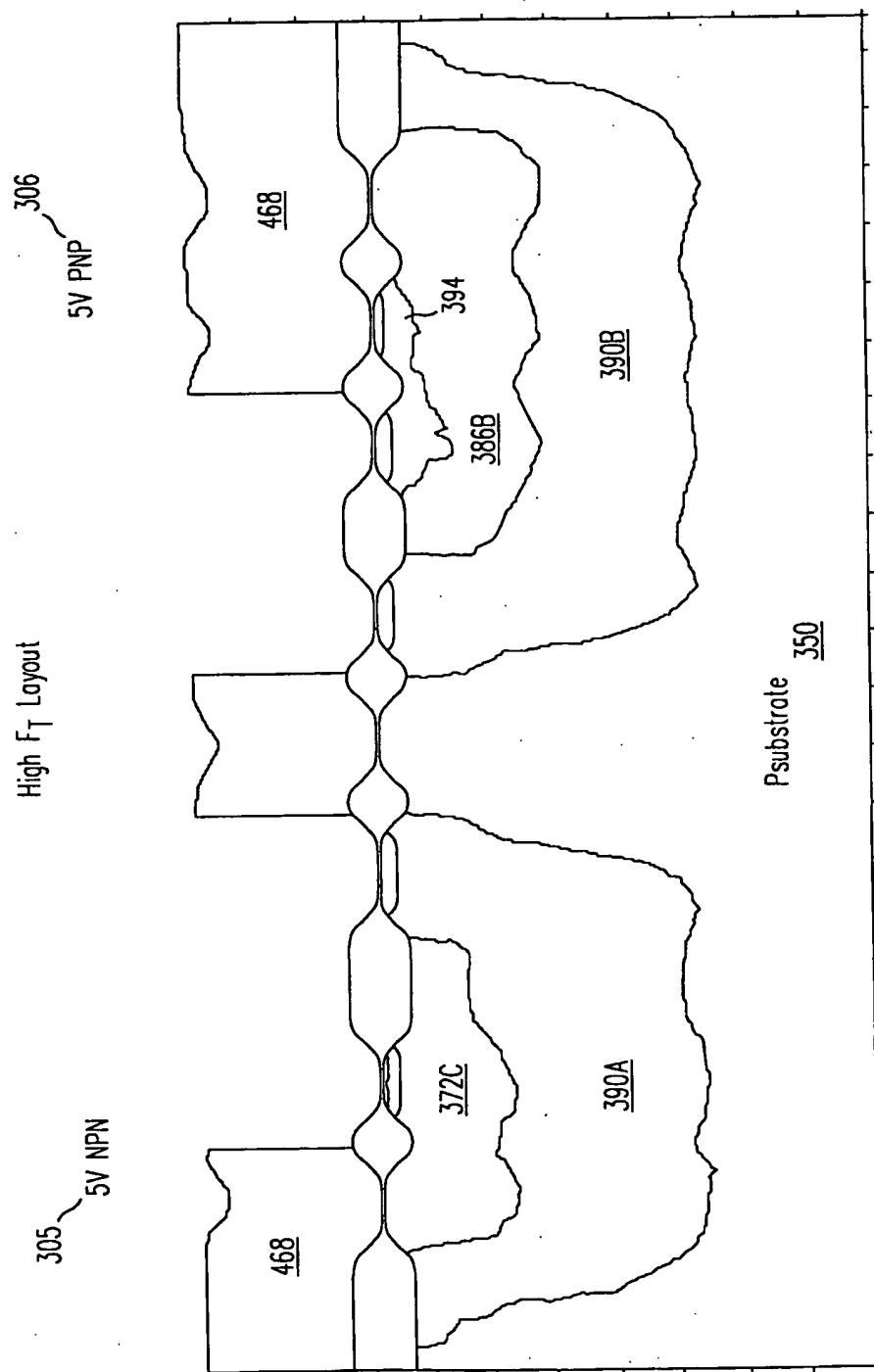
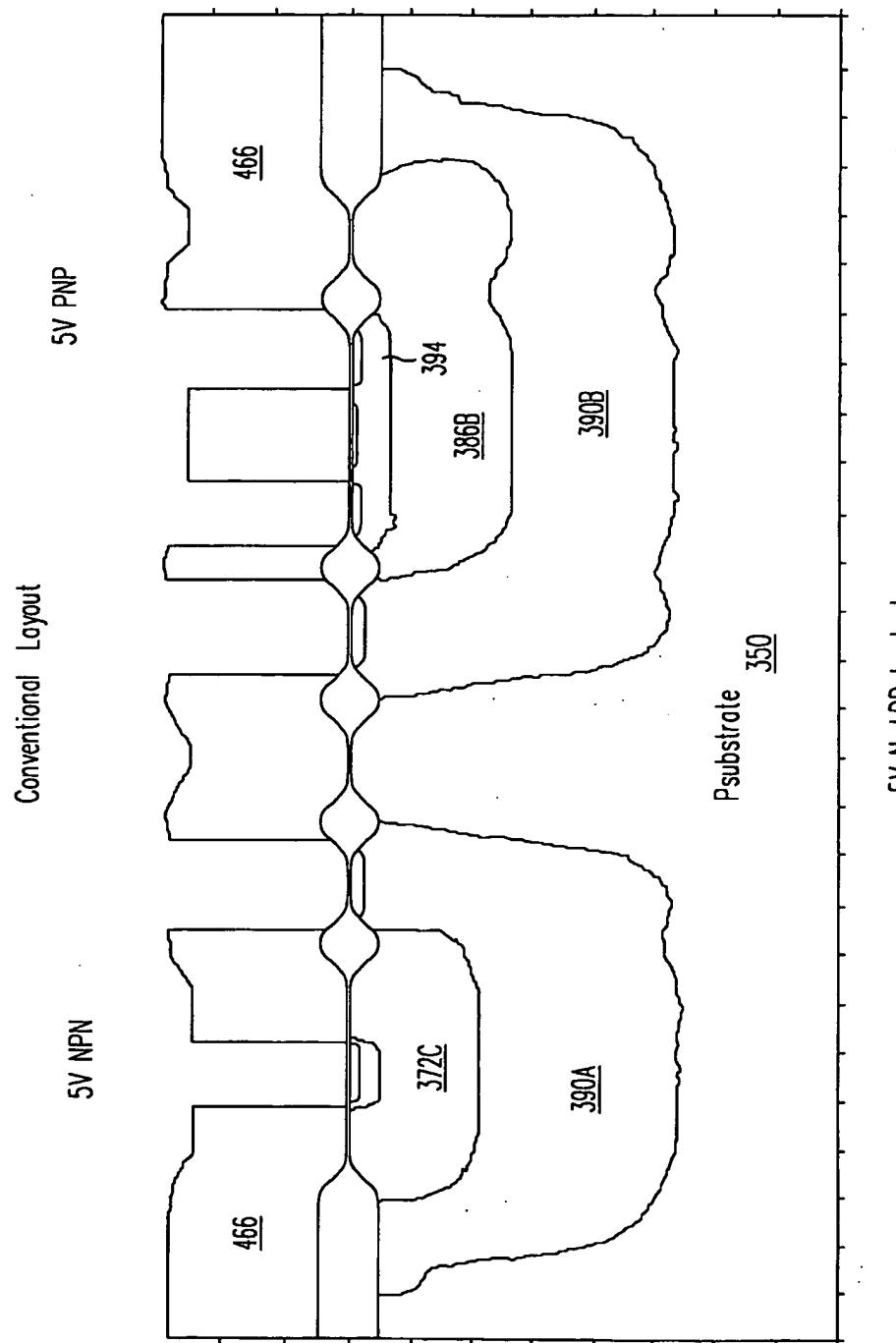
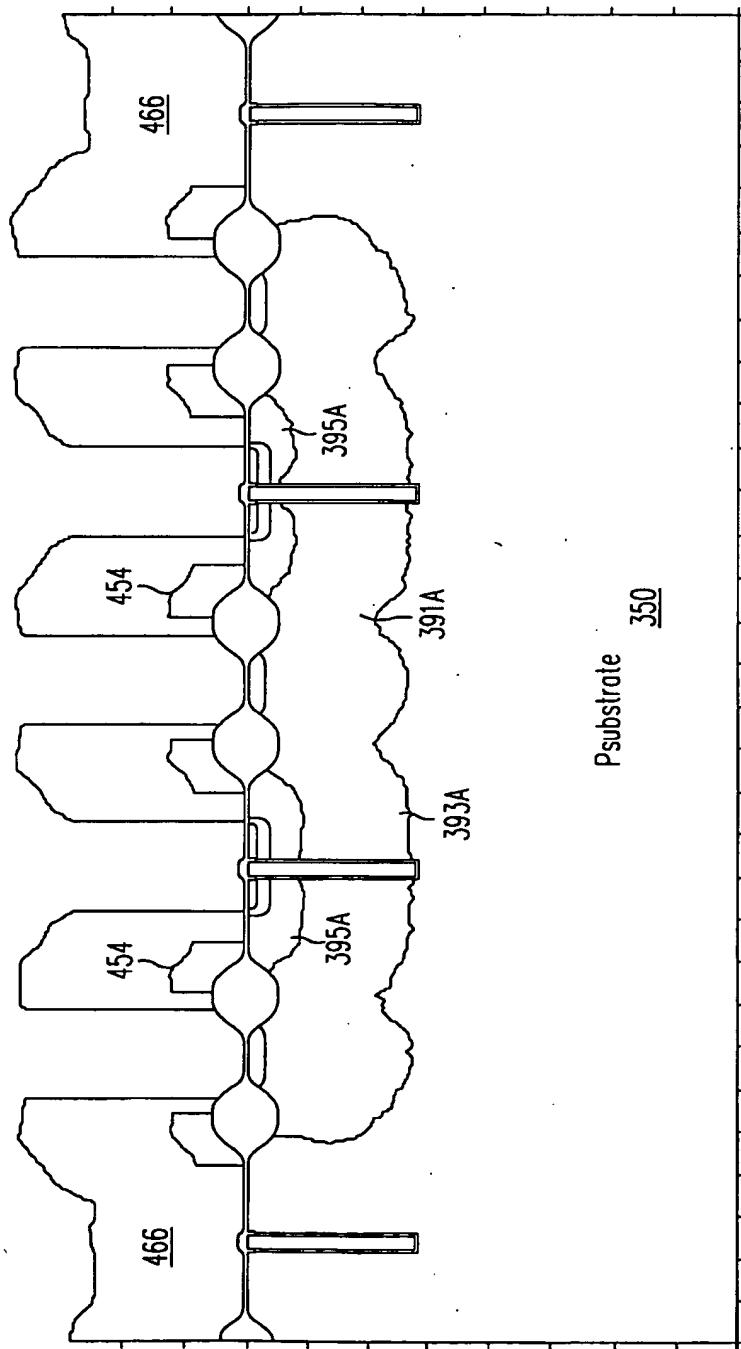


FIG. 60B



5V N-LOD Implant
FIG. 60C

30V Lateral French DMOS — 308



5V N-LDD implant

FIG. 60D

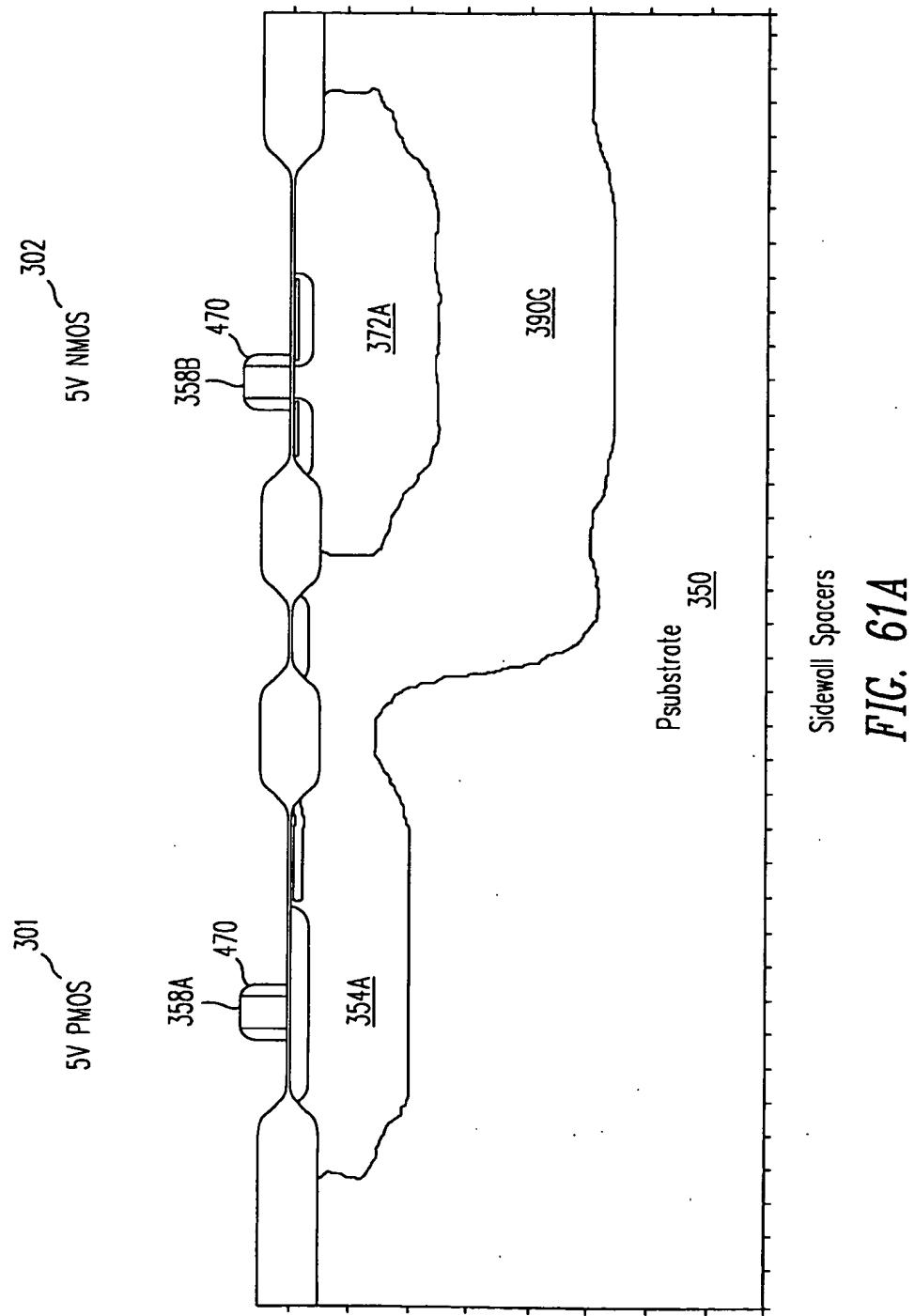


FIG. 61A

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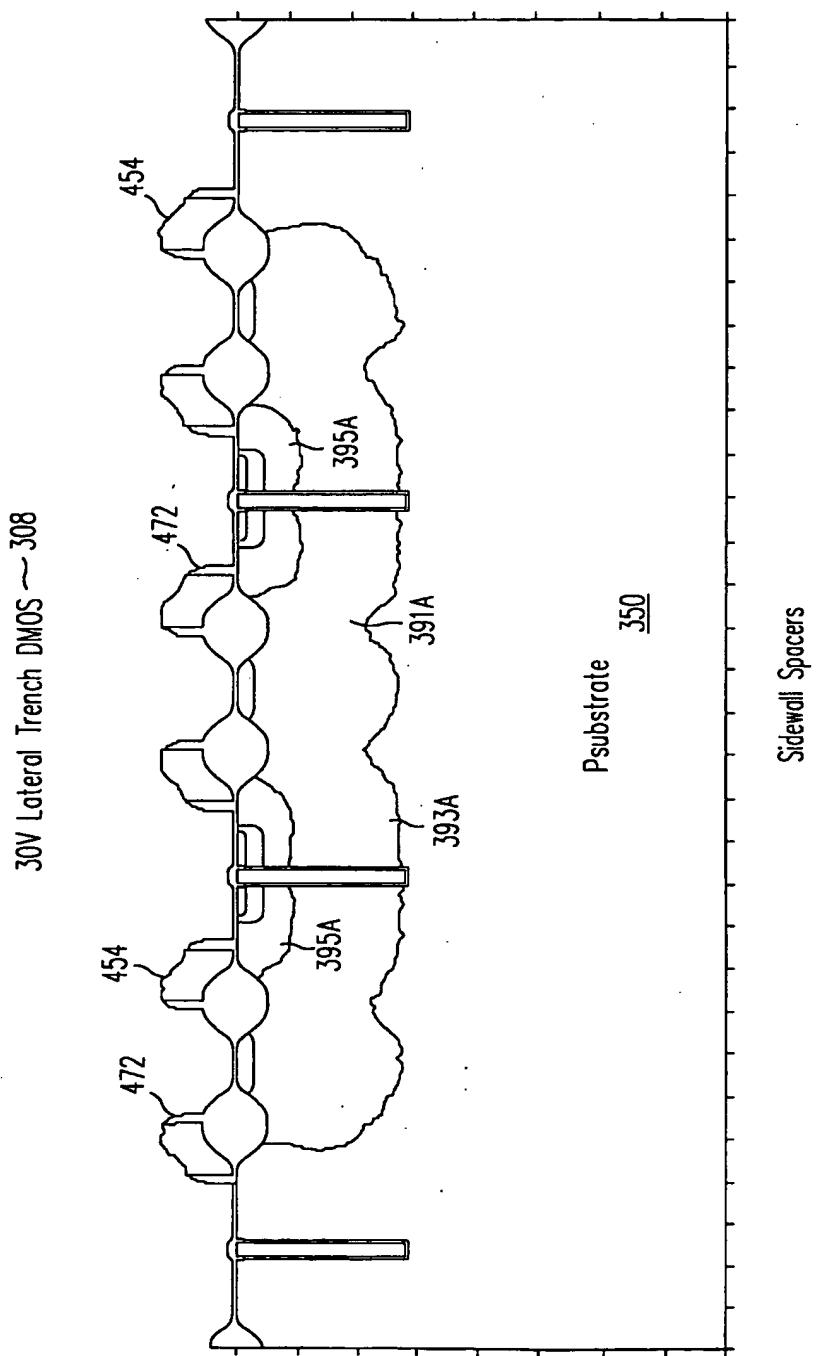
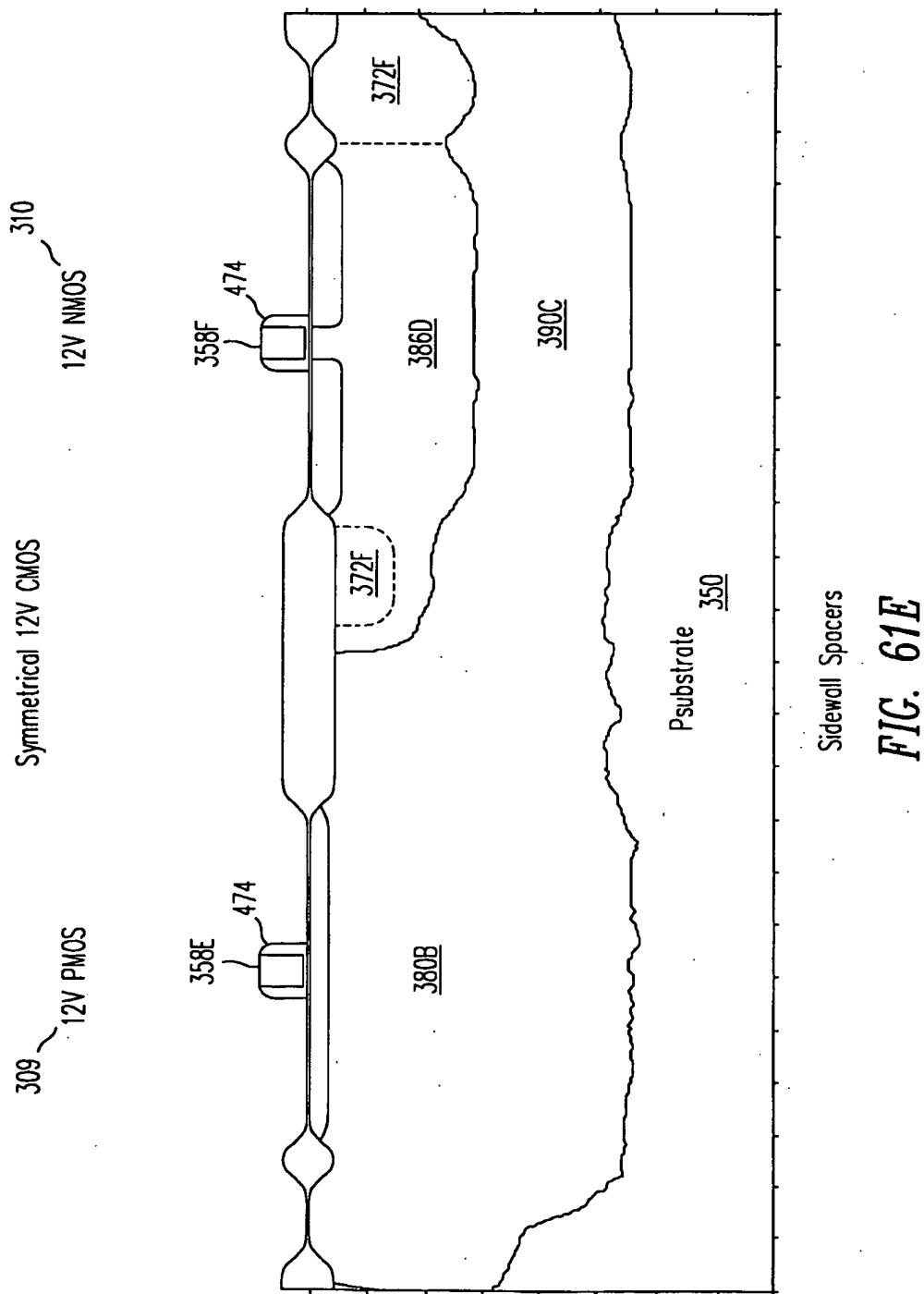


FIG. 61D

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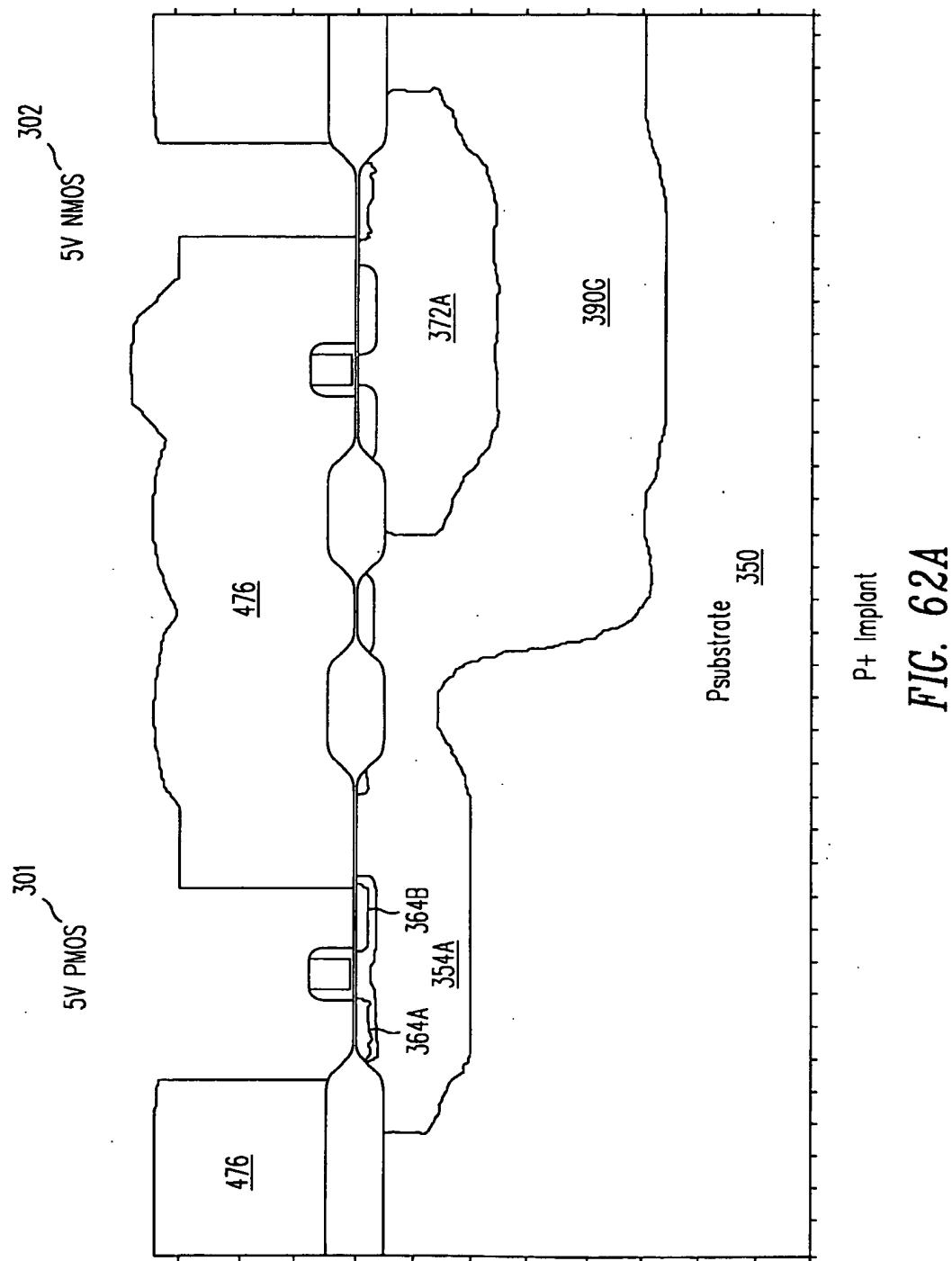


FIG. 62A

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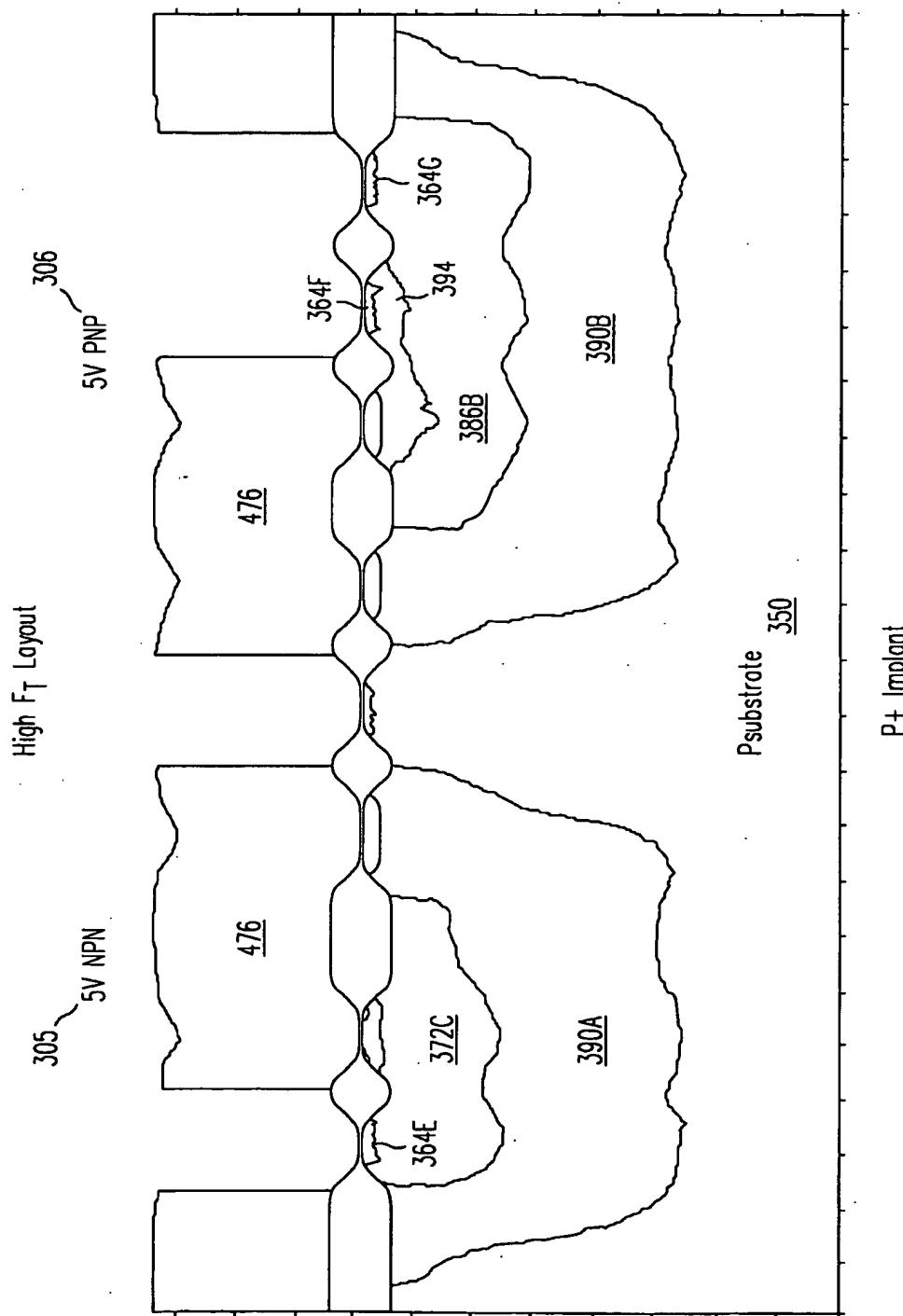
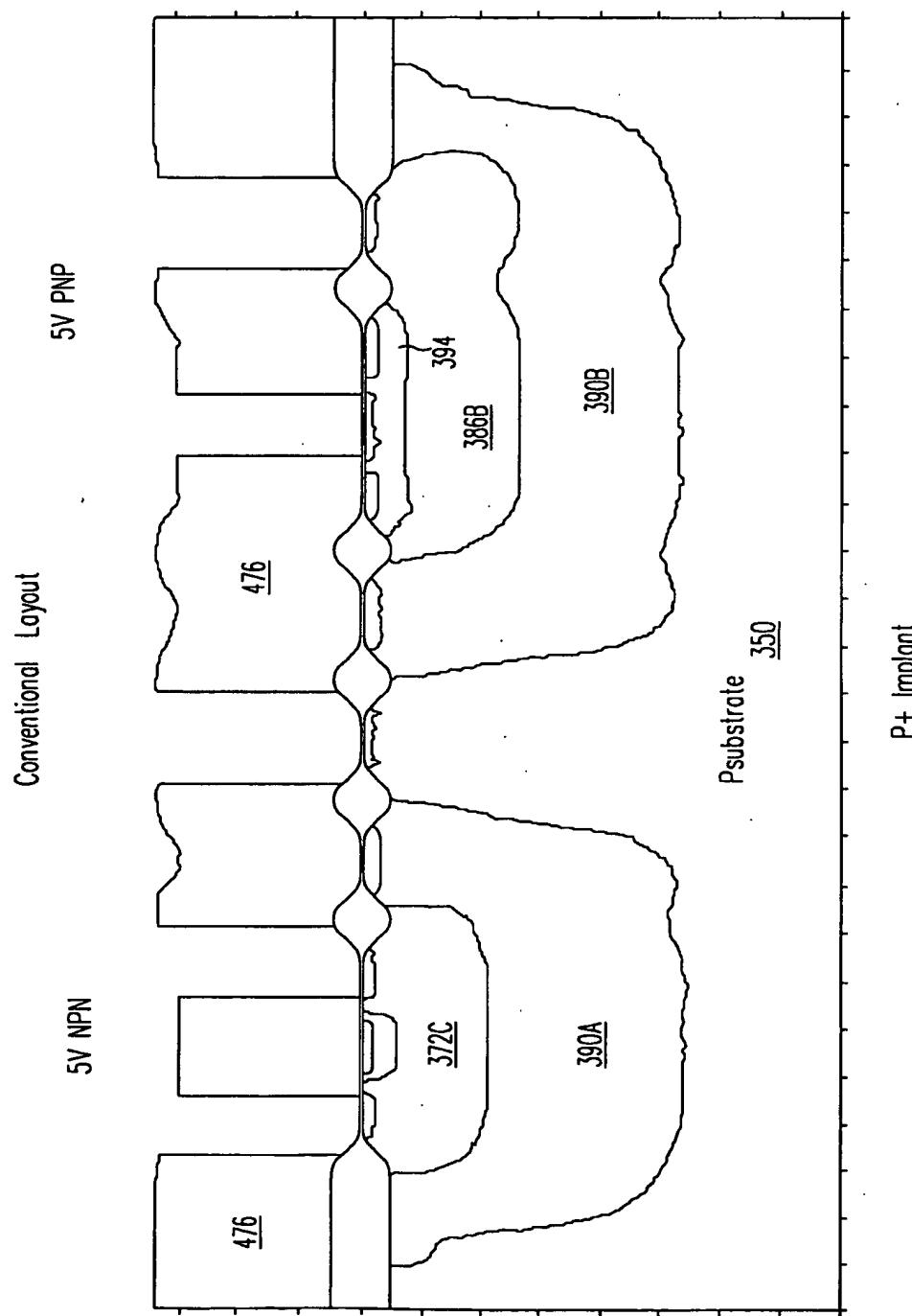


FIG. 62B

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P+ implant
FIG. 62C

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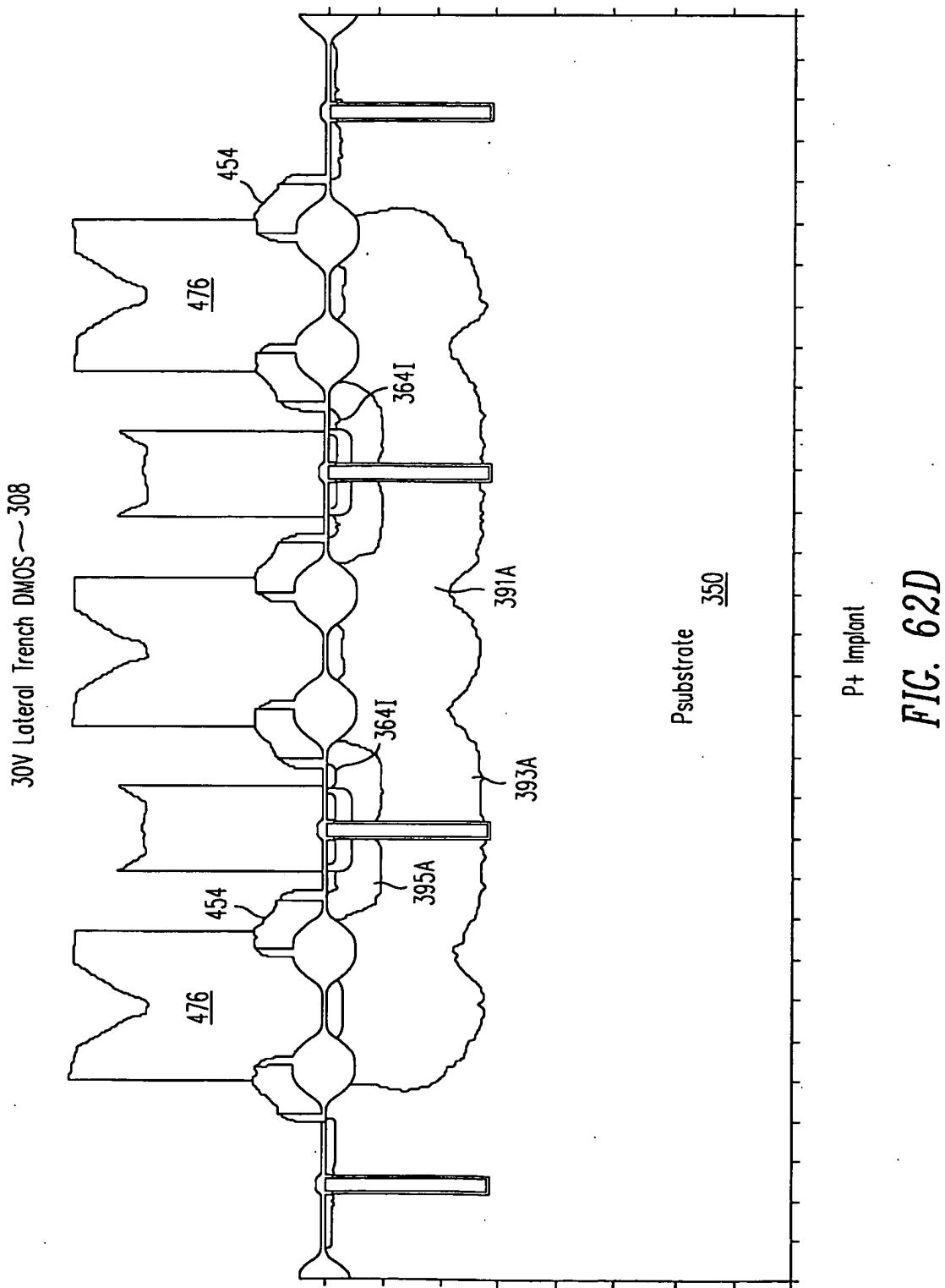
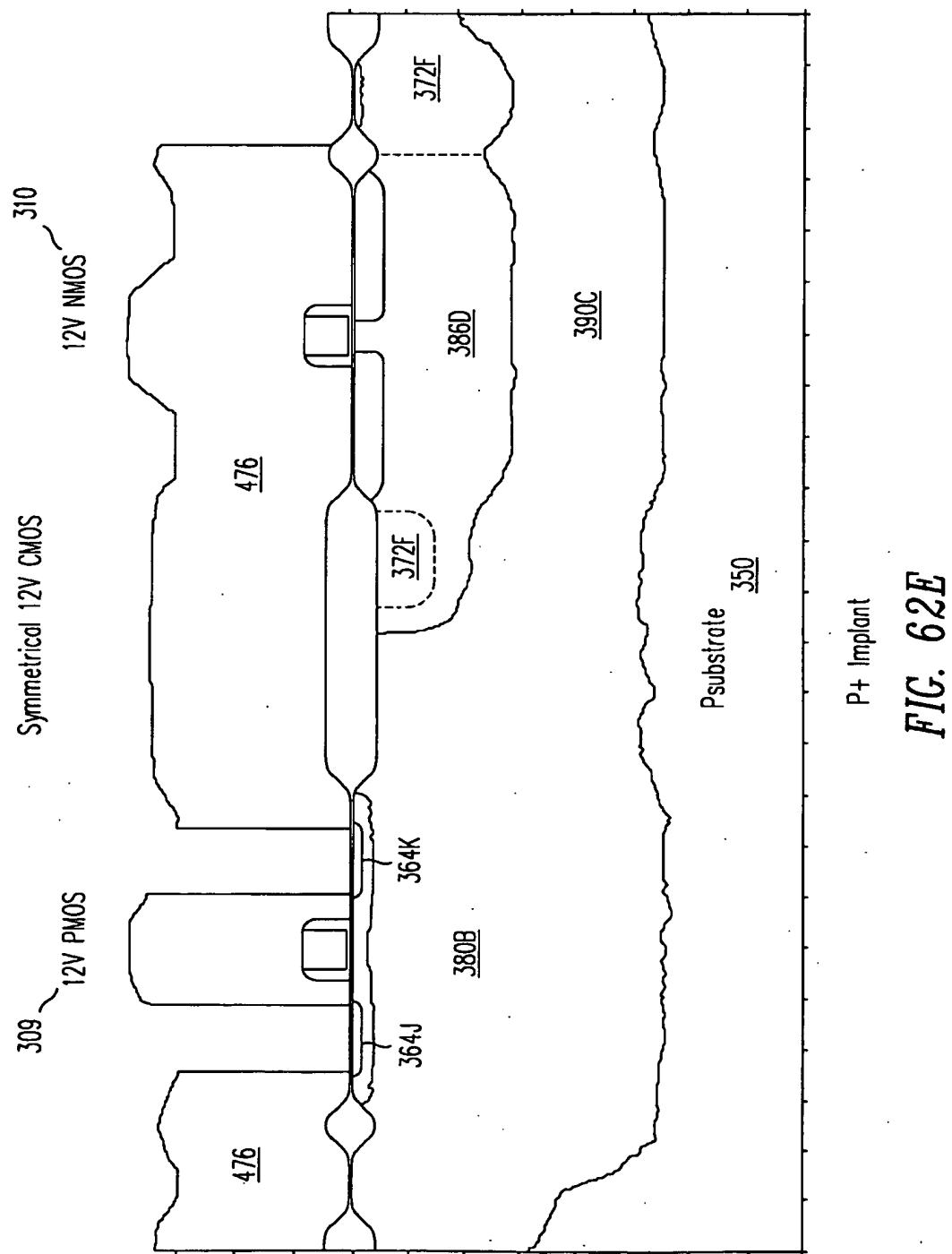


FIG. 62D

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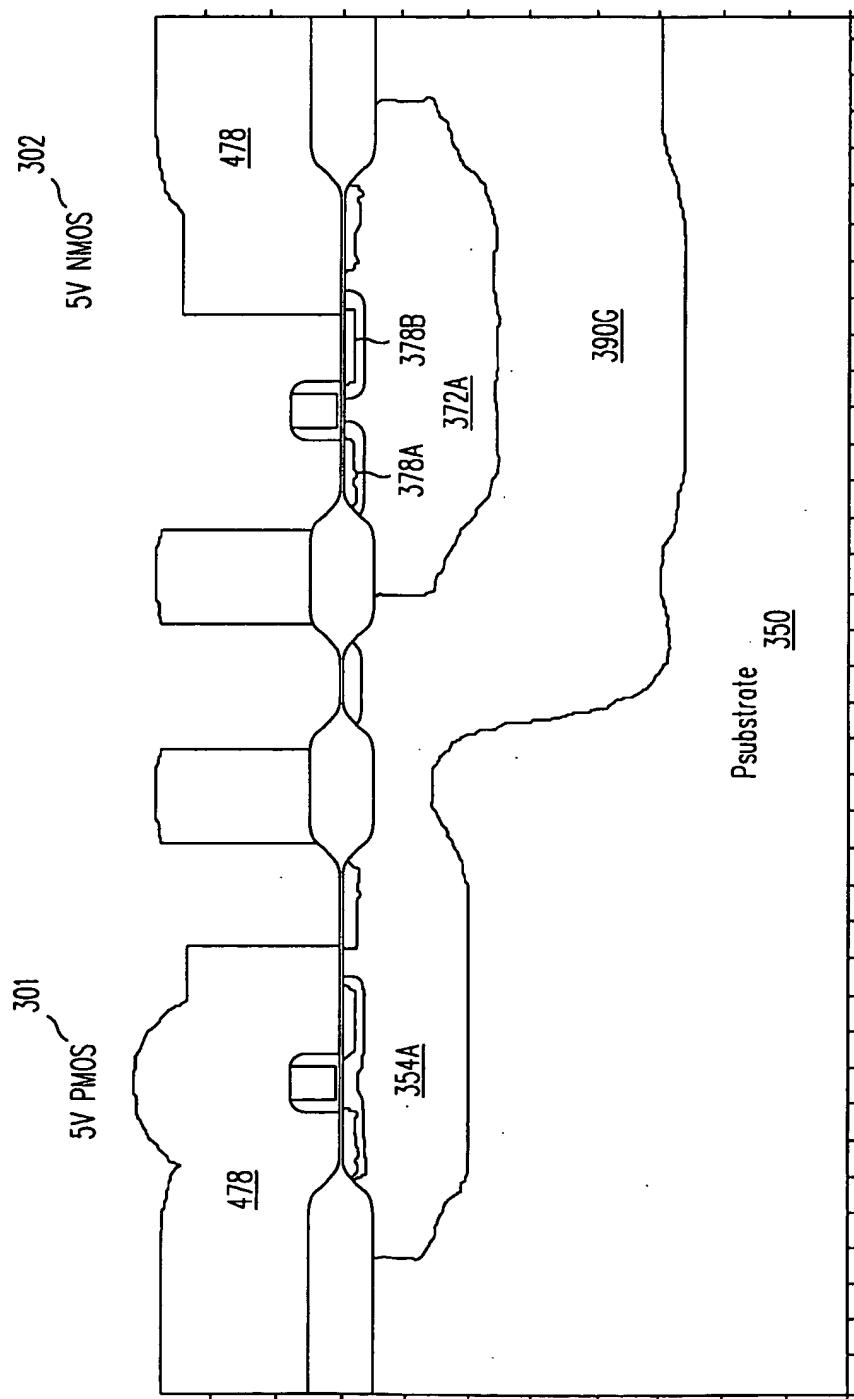
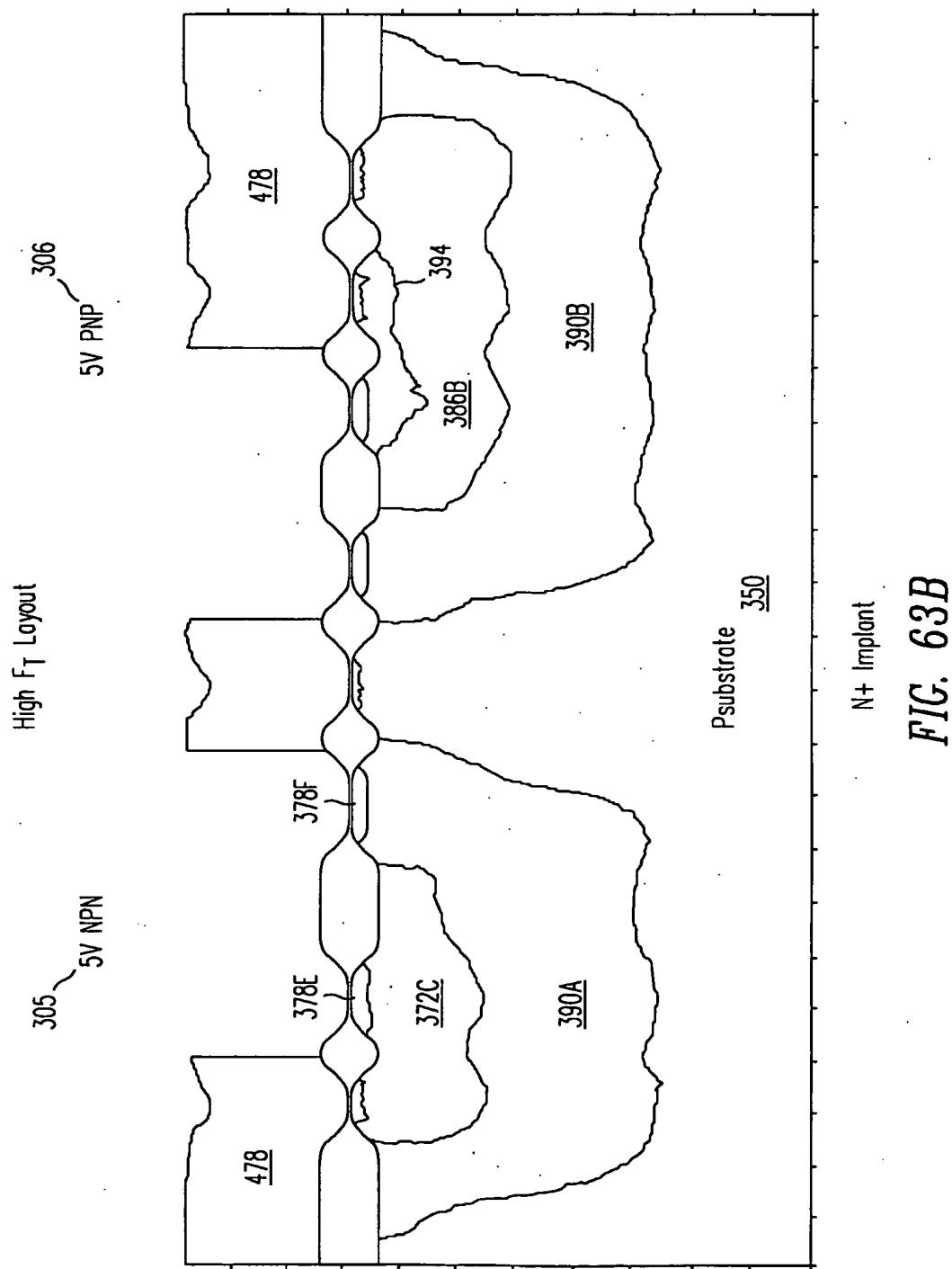
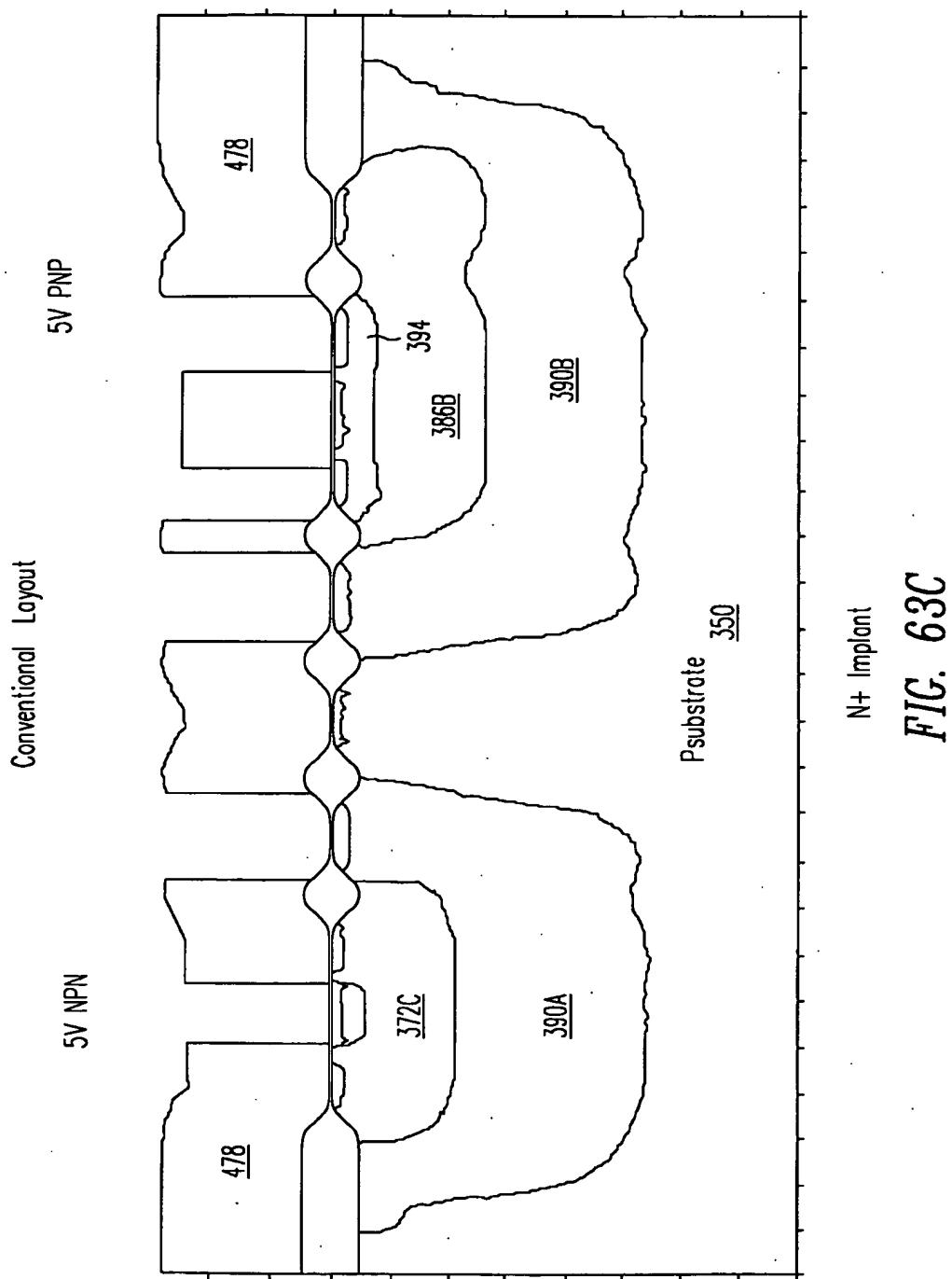


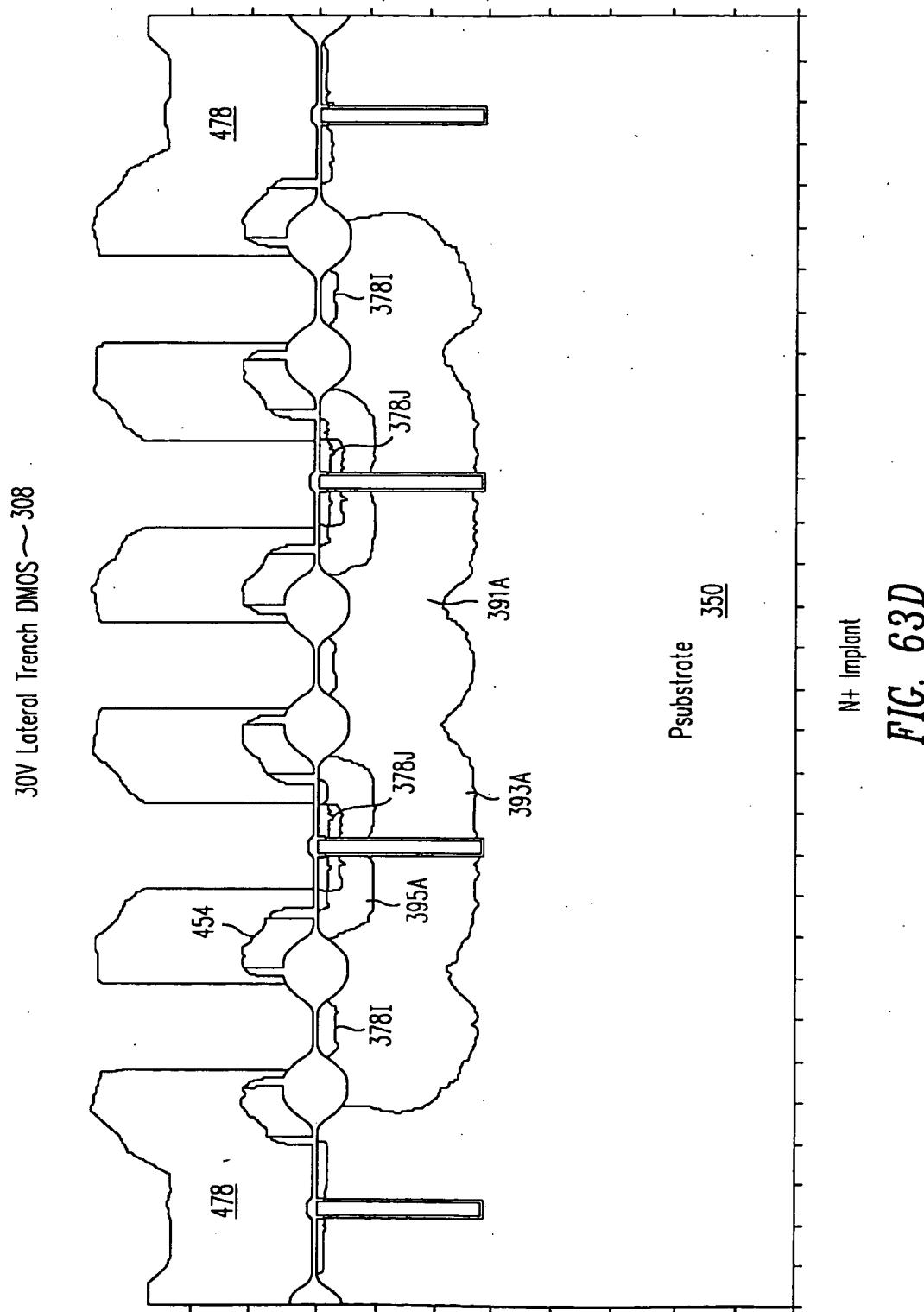
FIG. 634

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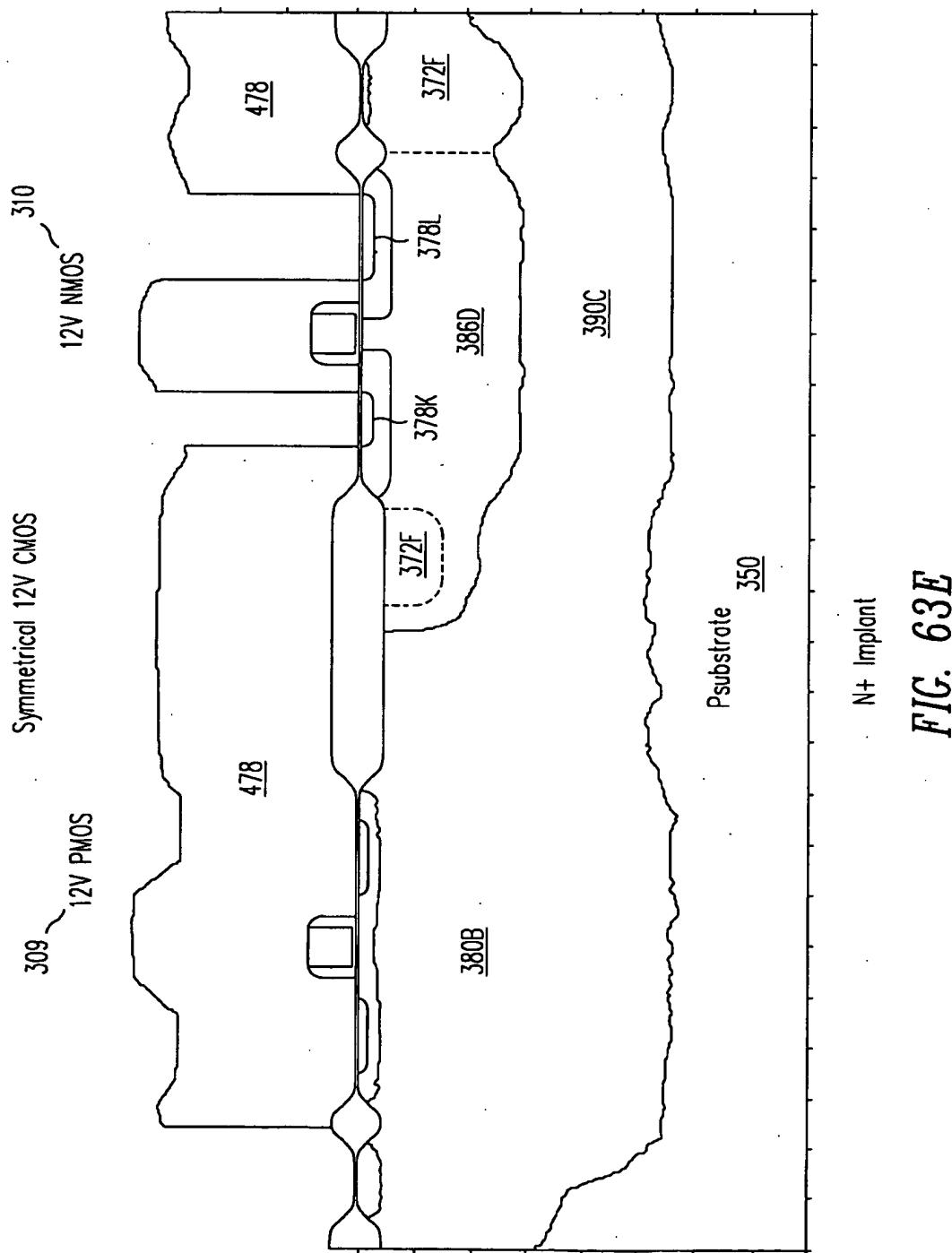




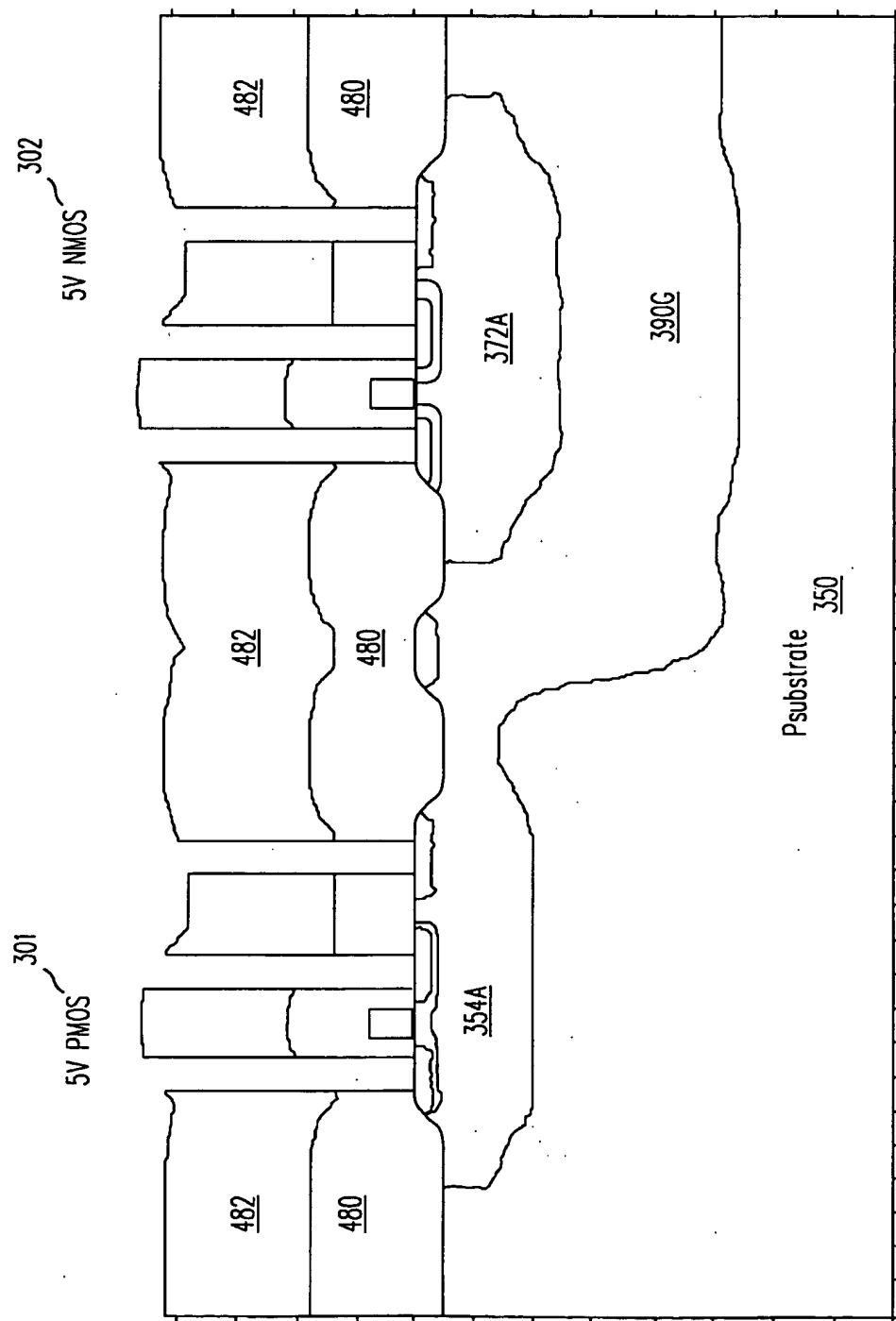
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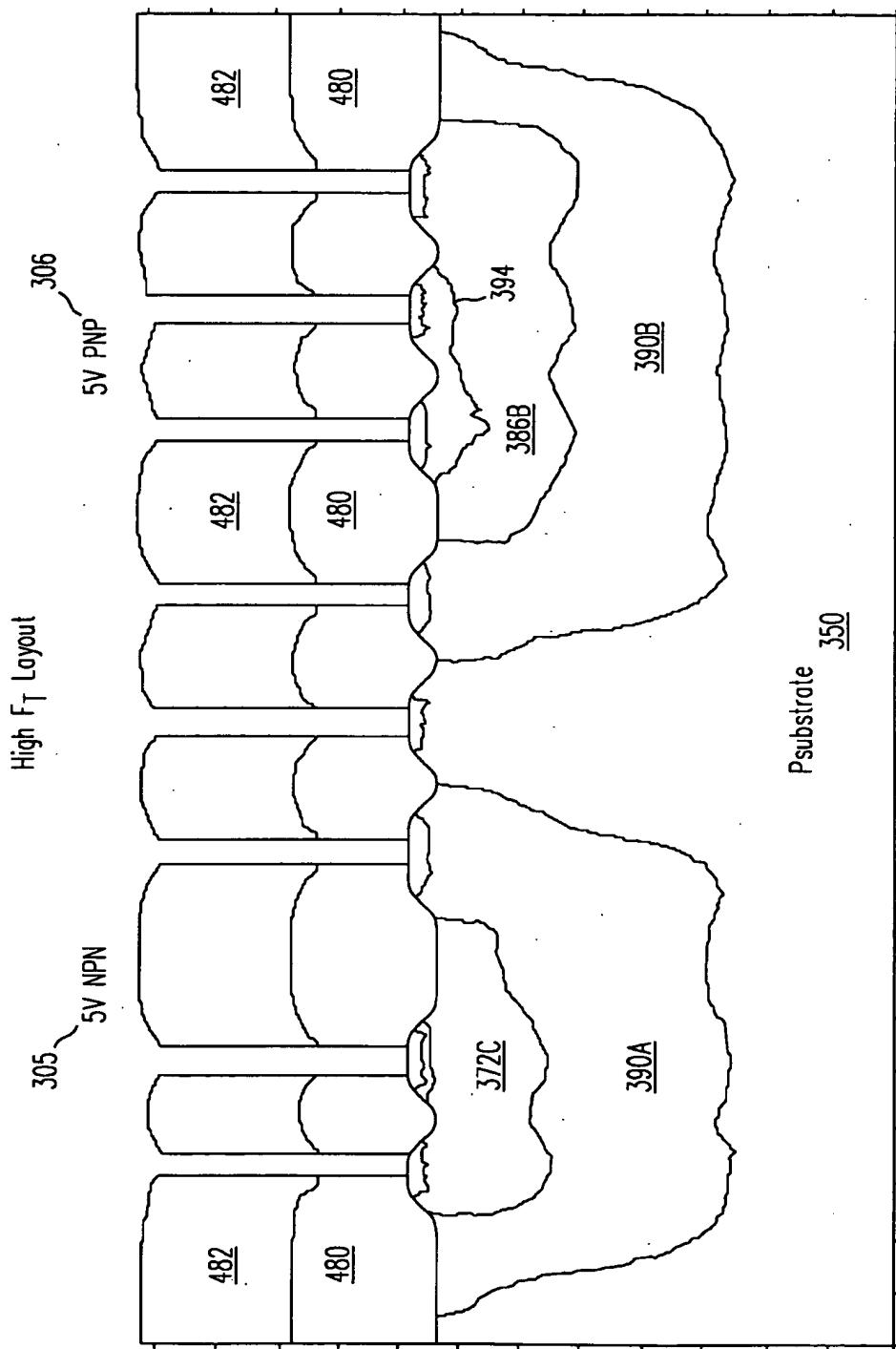


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Interlayer Dielectric Deposition and Etch

FIG. 64A



Interlayer Dielectric Deposition and Etch

FIG. 64B

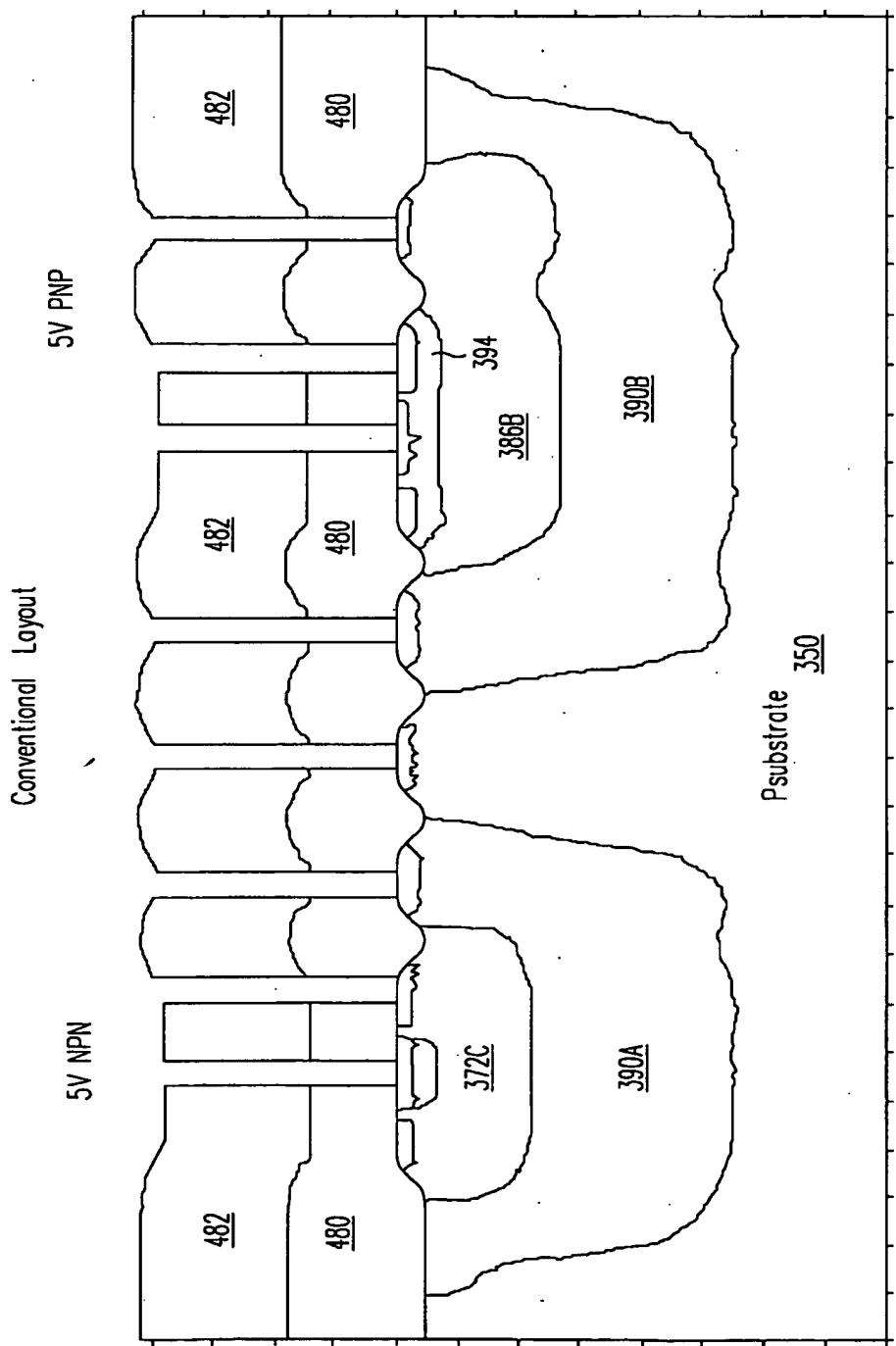


FIG. 64C

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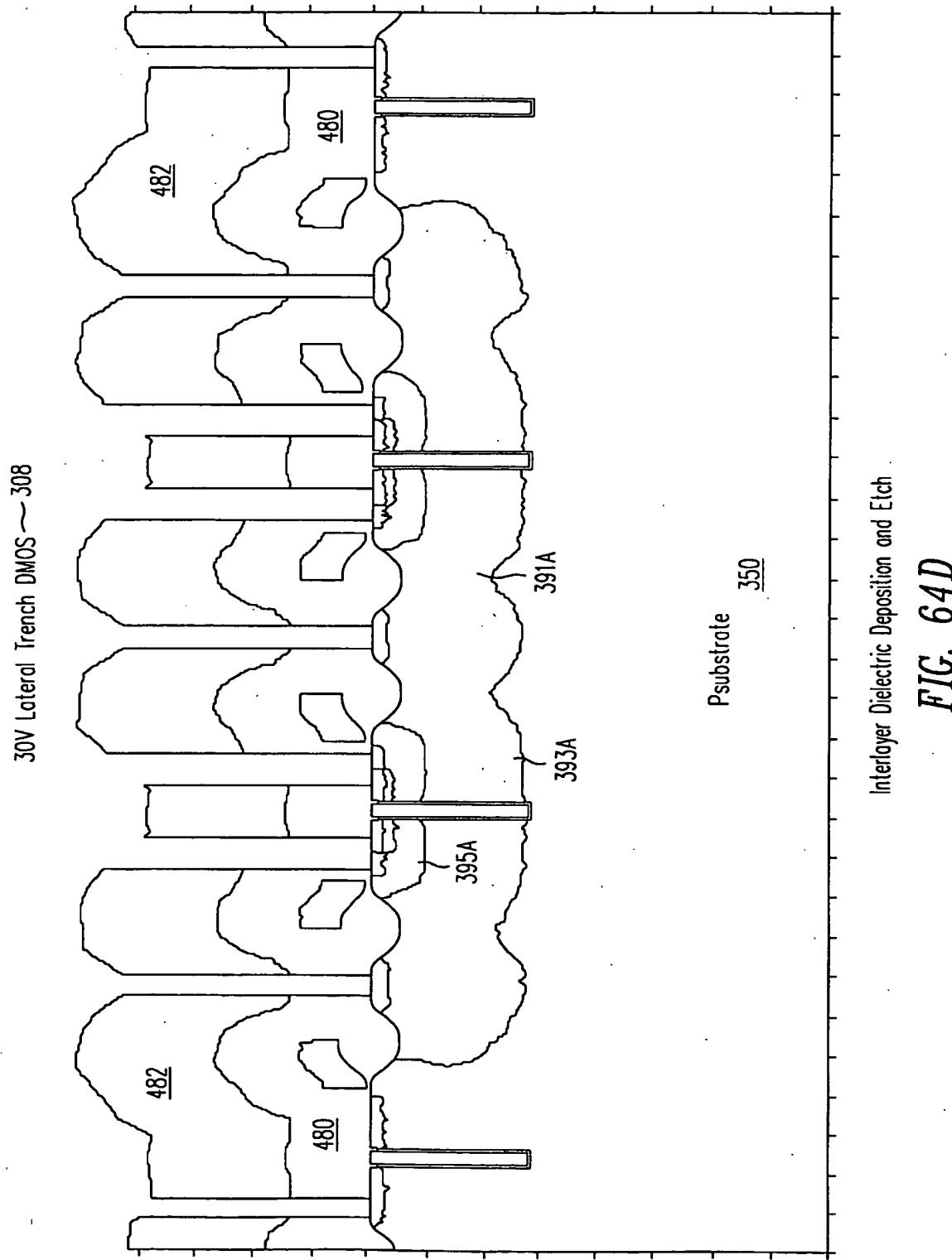
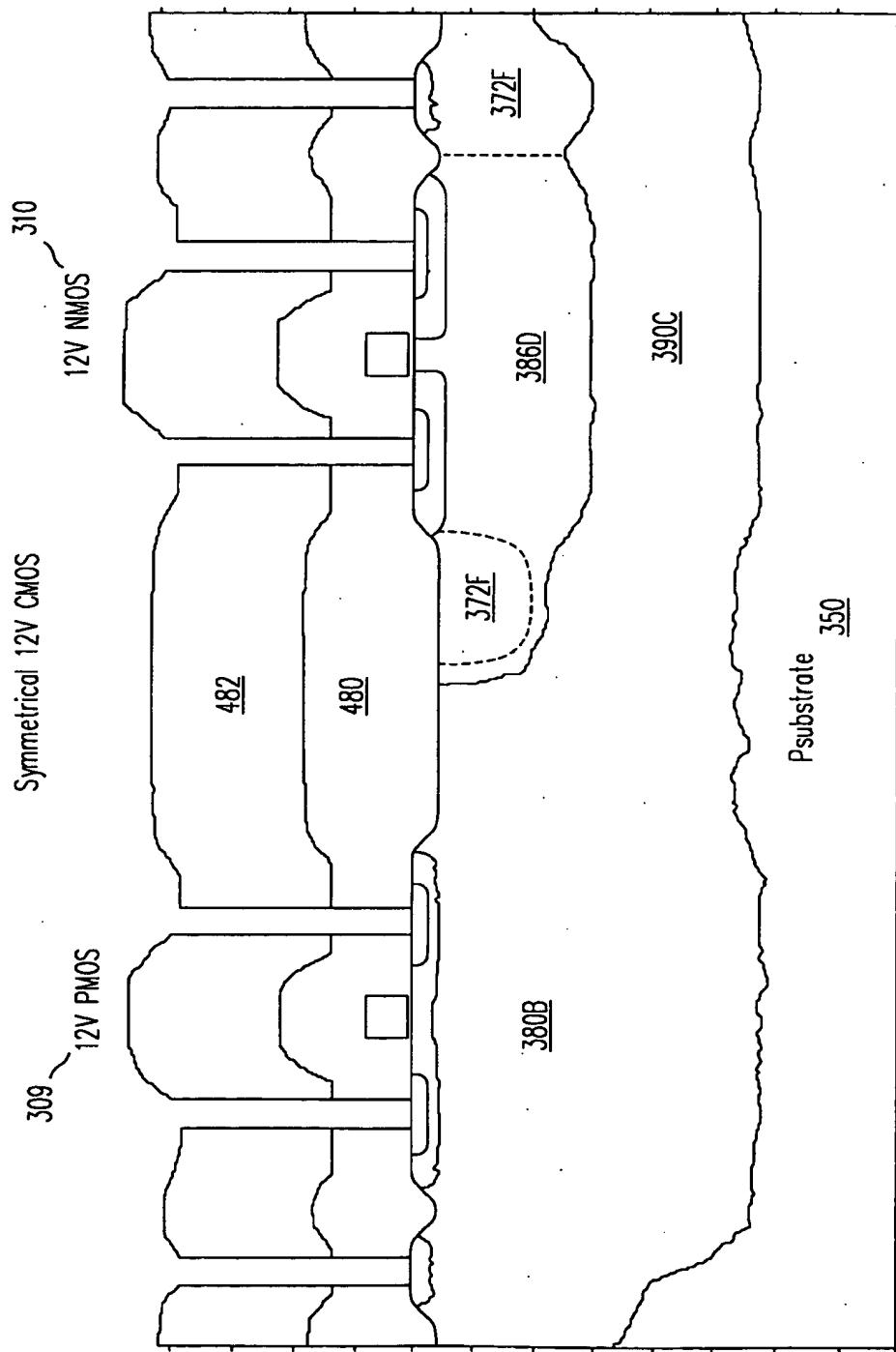


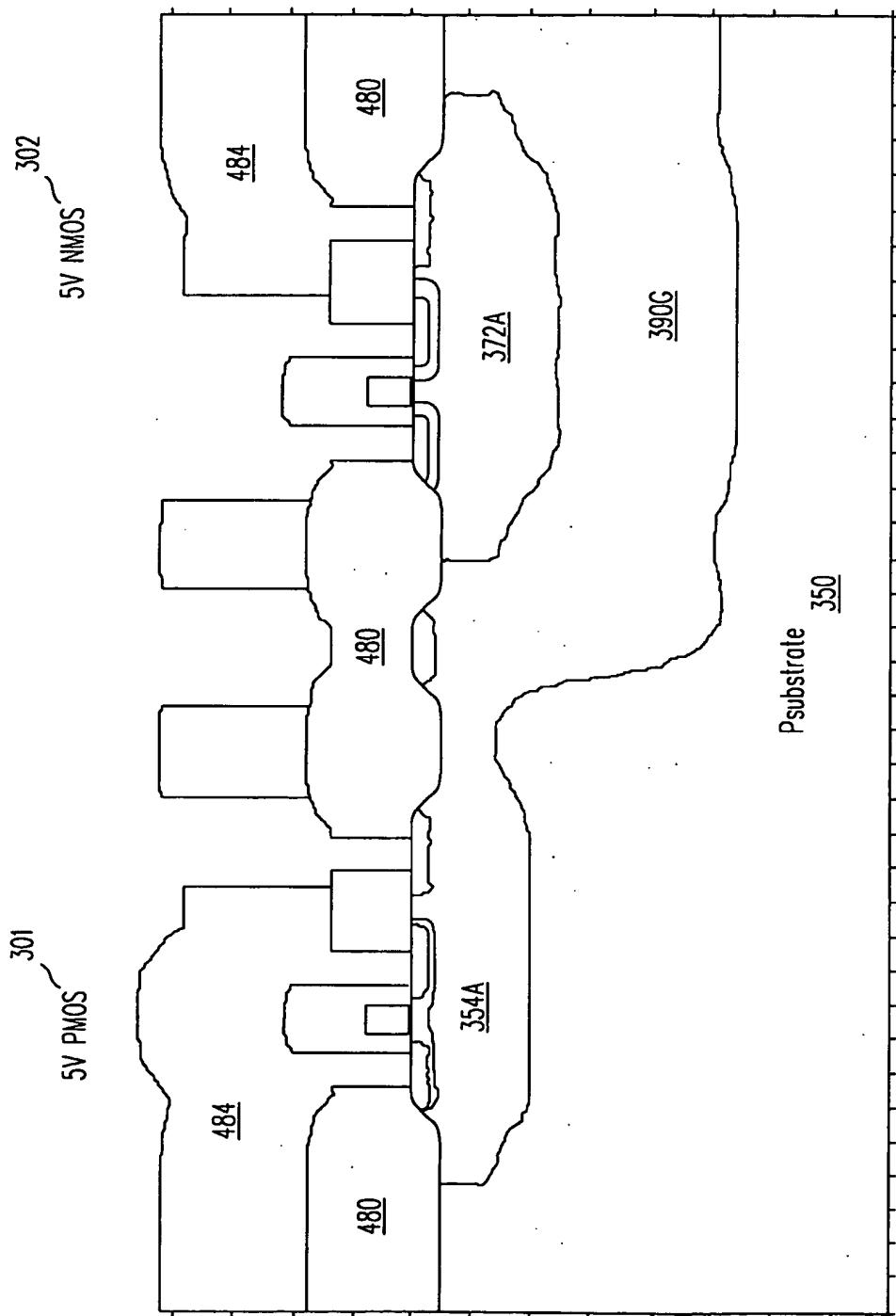
FIG. 64D



Interlayer Dielectric Deposition and Etch

FIG. 64E

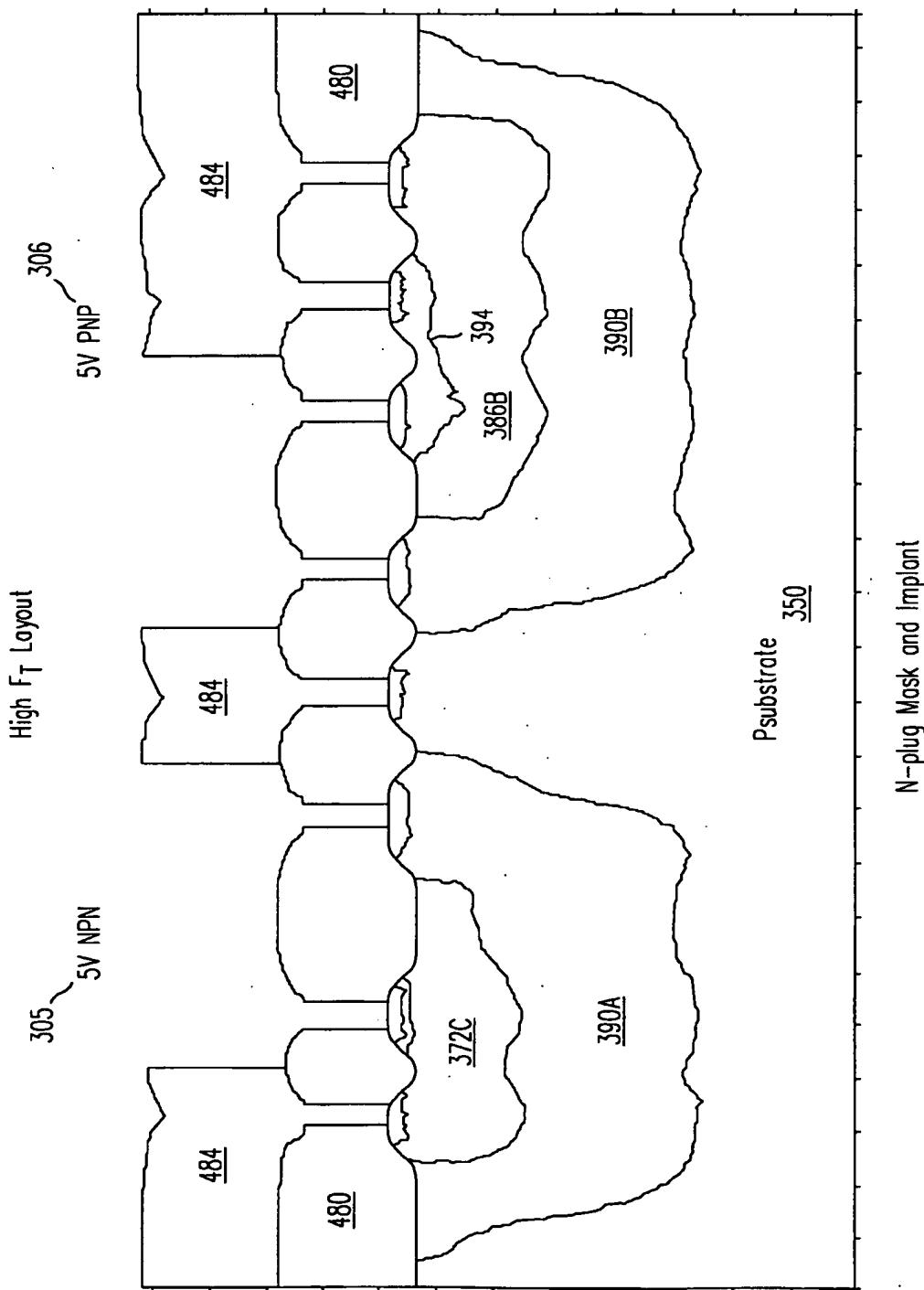
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N-plug Mask and Implant

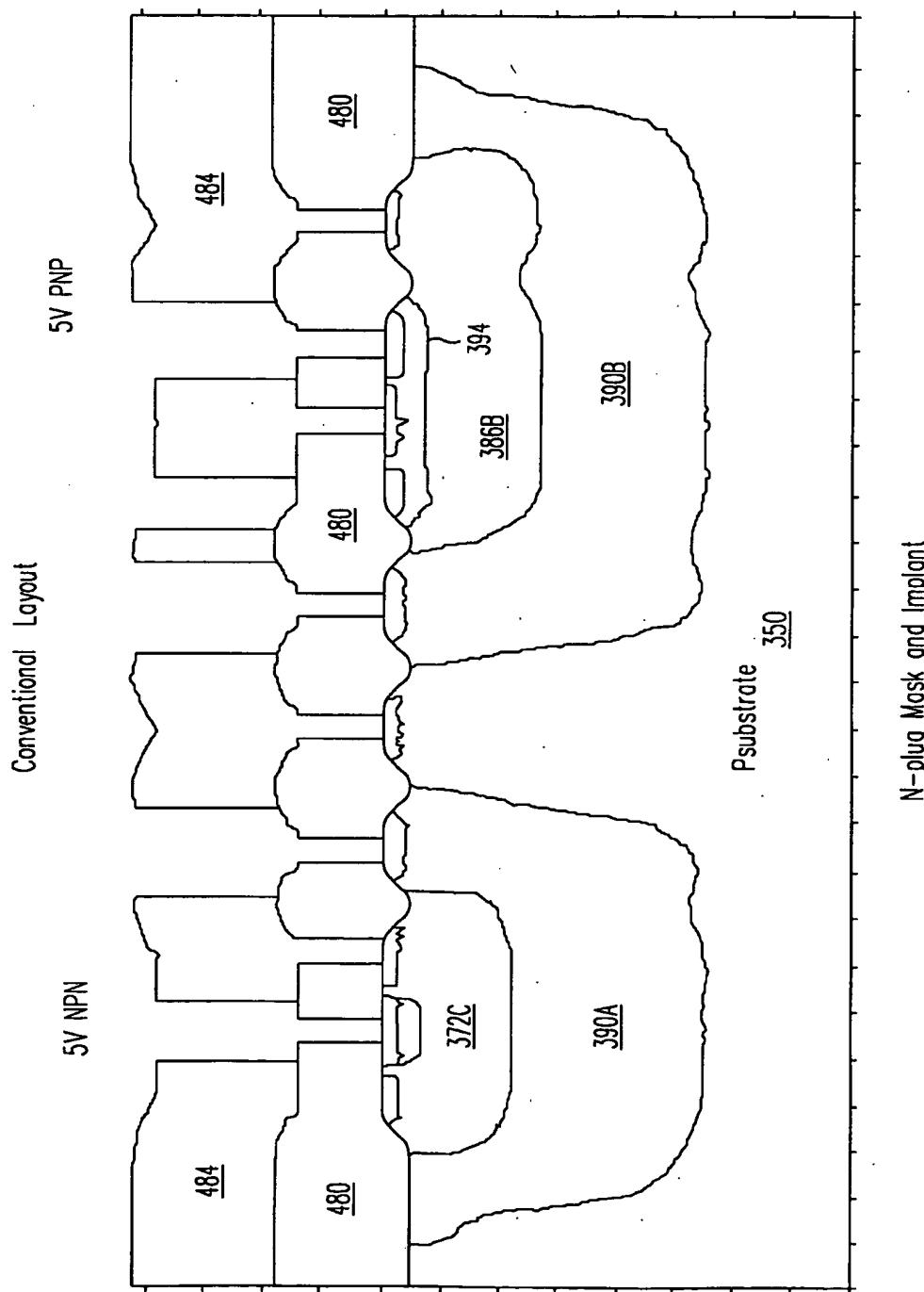
FIG. 65A

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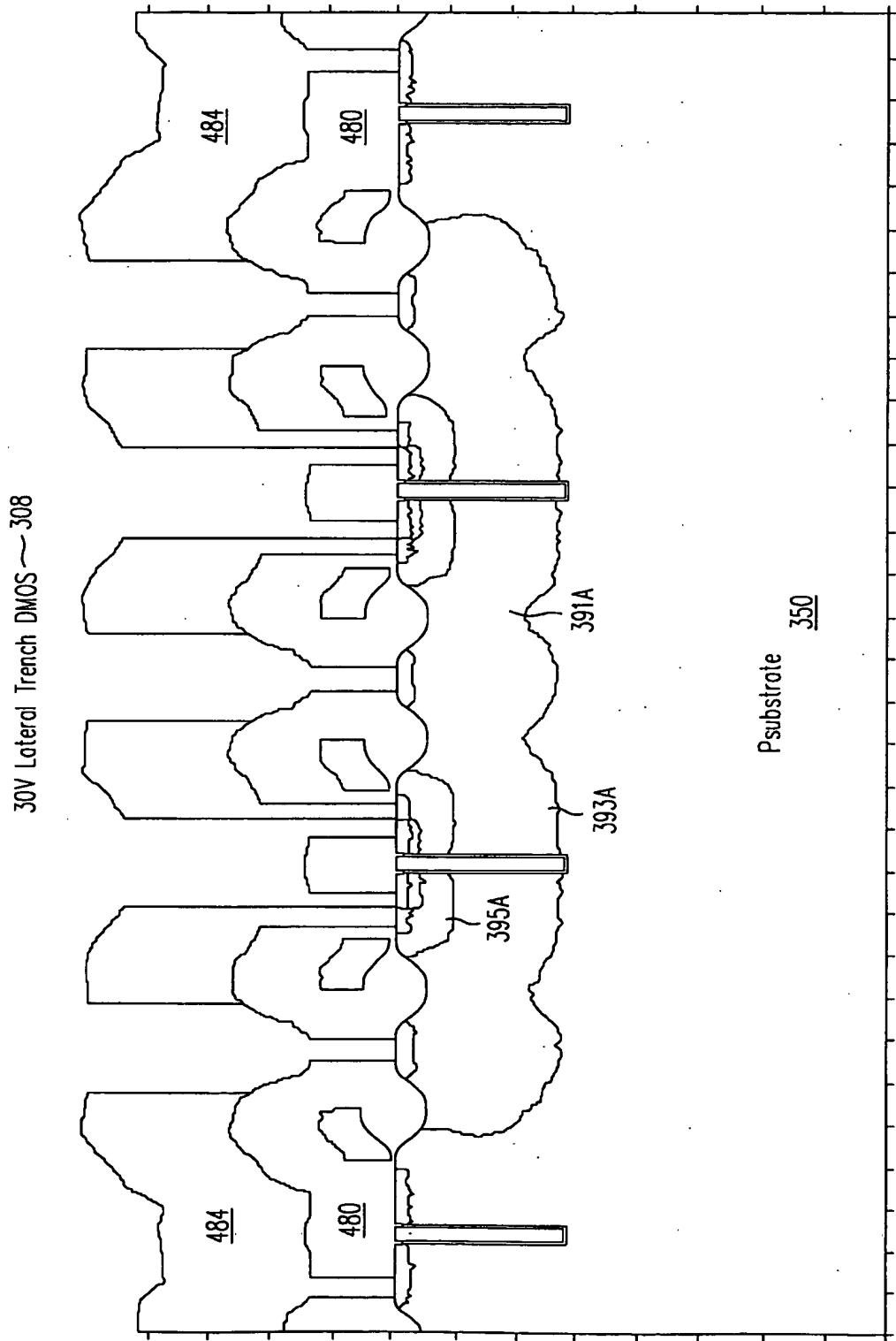
N-plug Mask and Implant

FIG. 65B



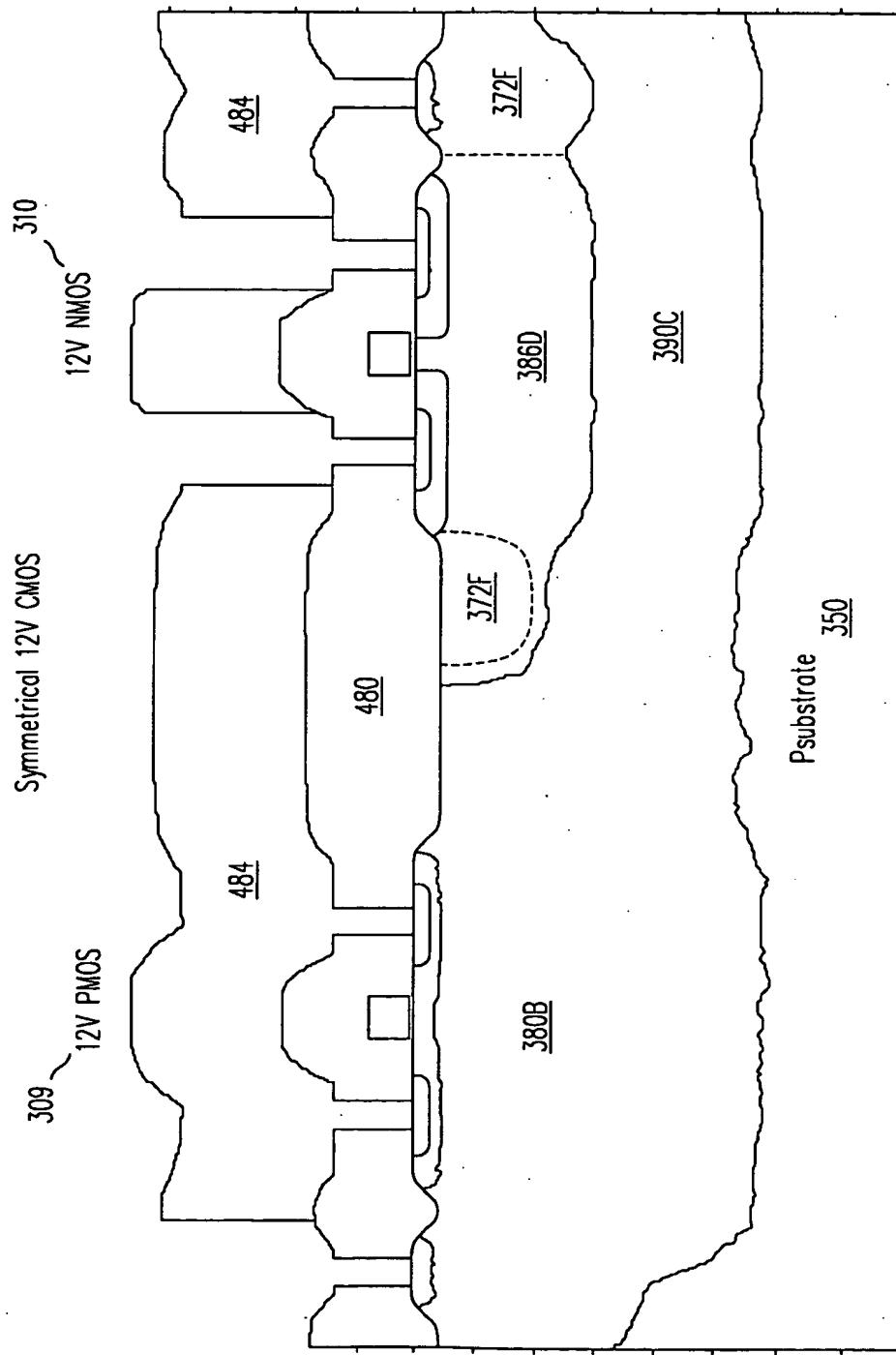
N-plug Mask and Implant
FIG. 65C

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N-plug Mask and Implant
FIG. 65D

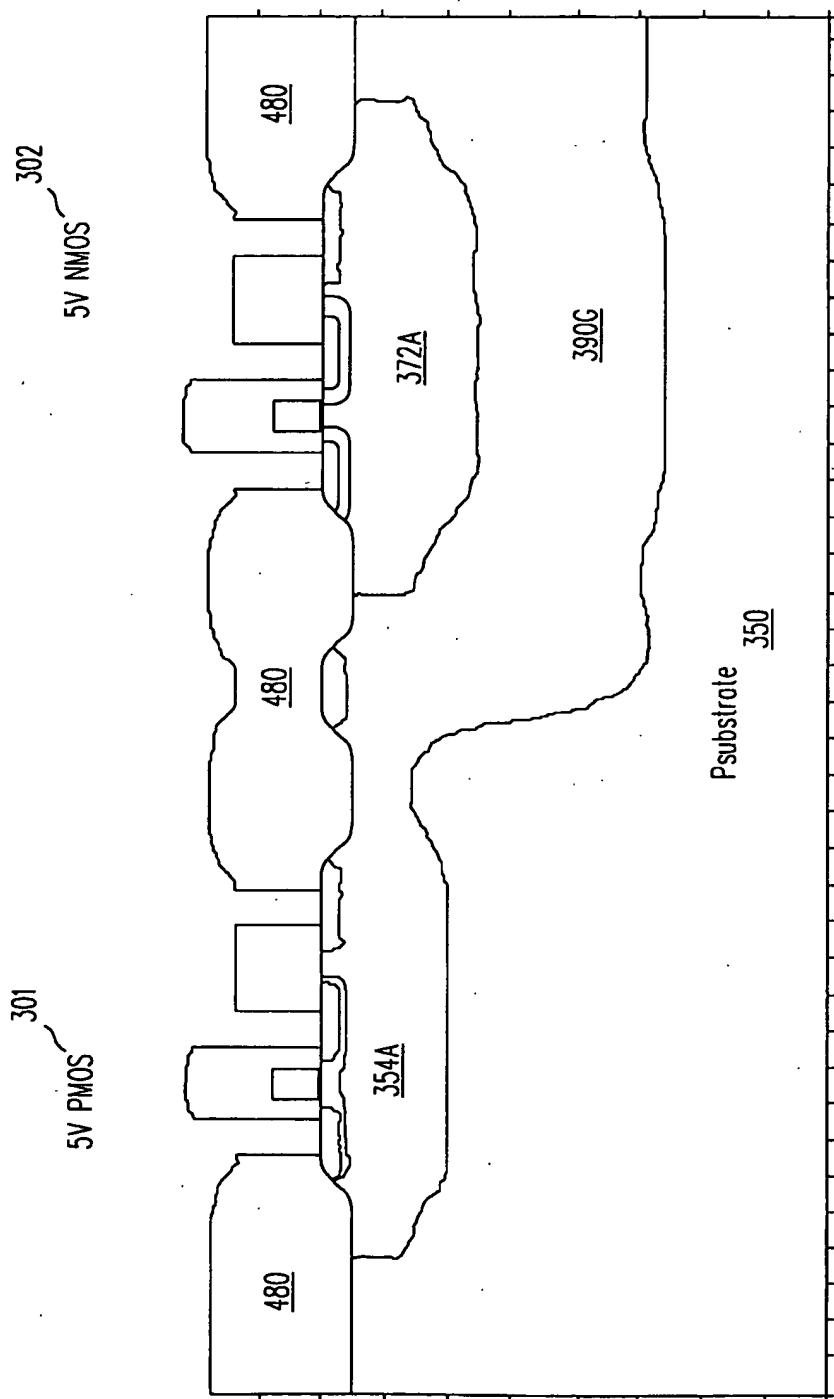
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N-plug Mask and Implant

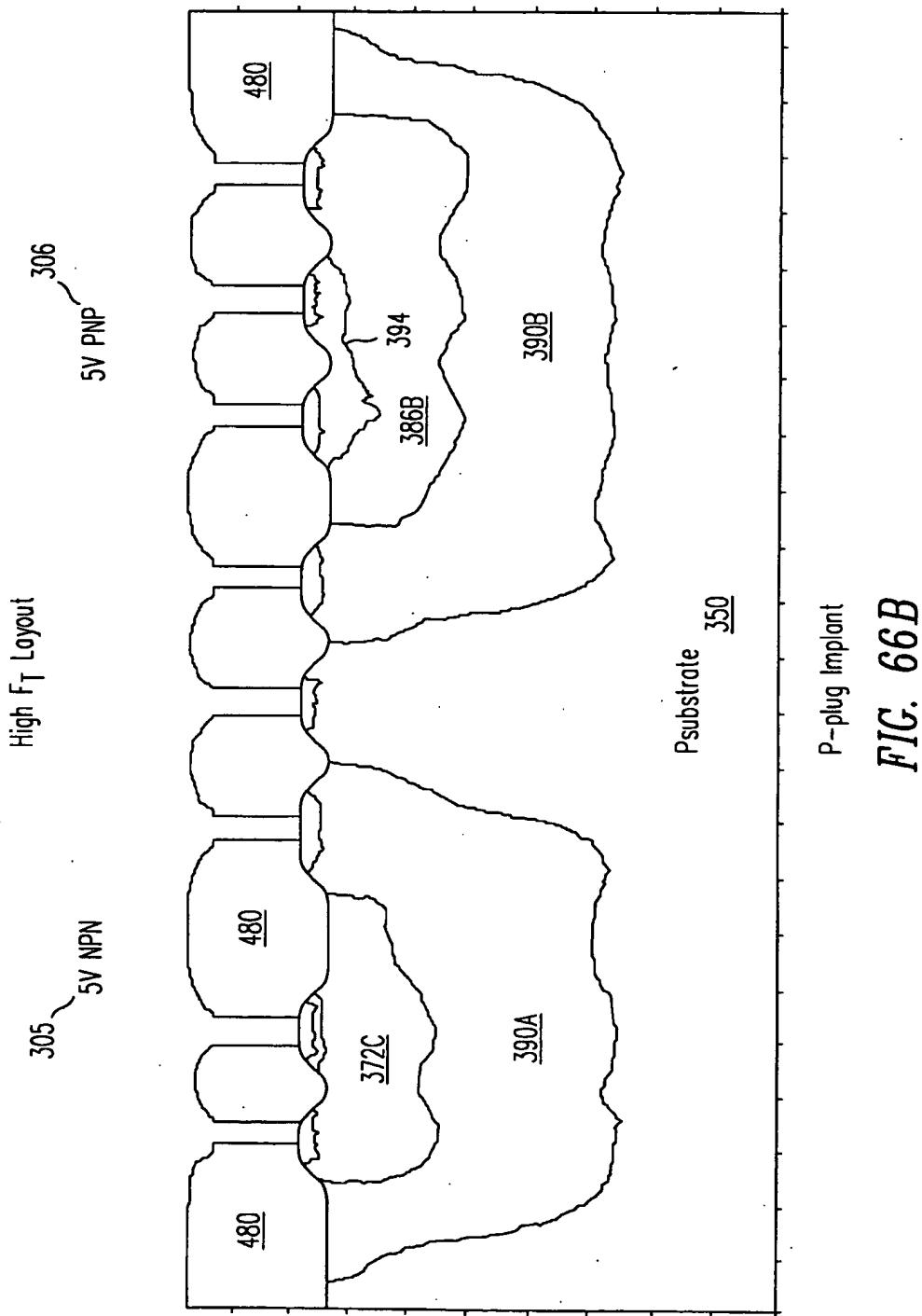
FIG. 65E

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P-plug Implant
FIG. 664

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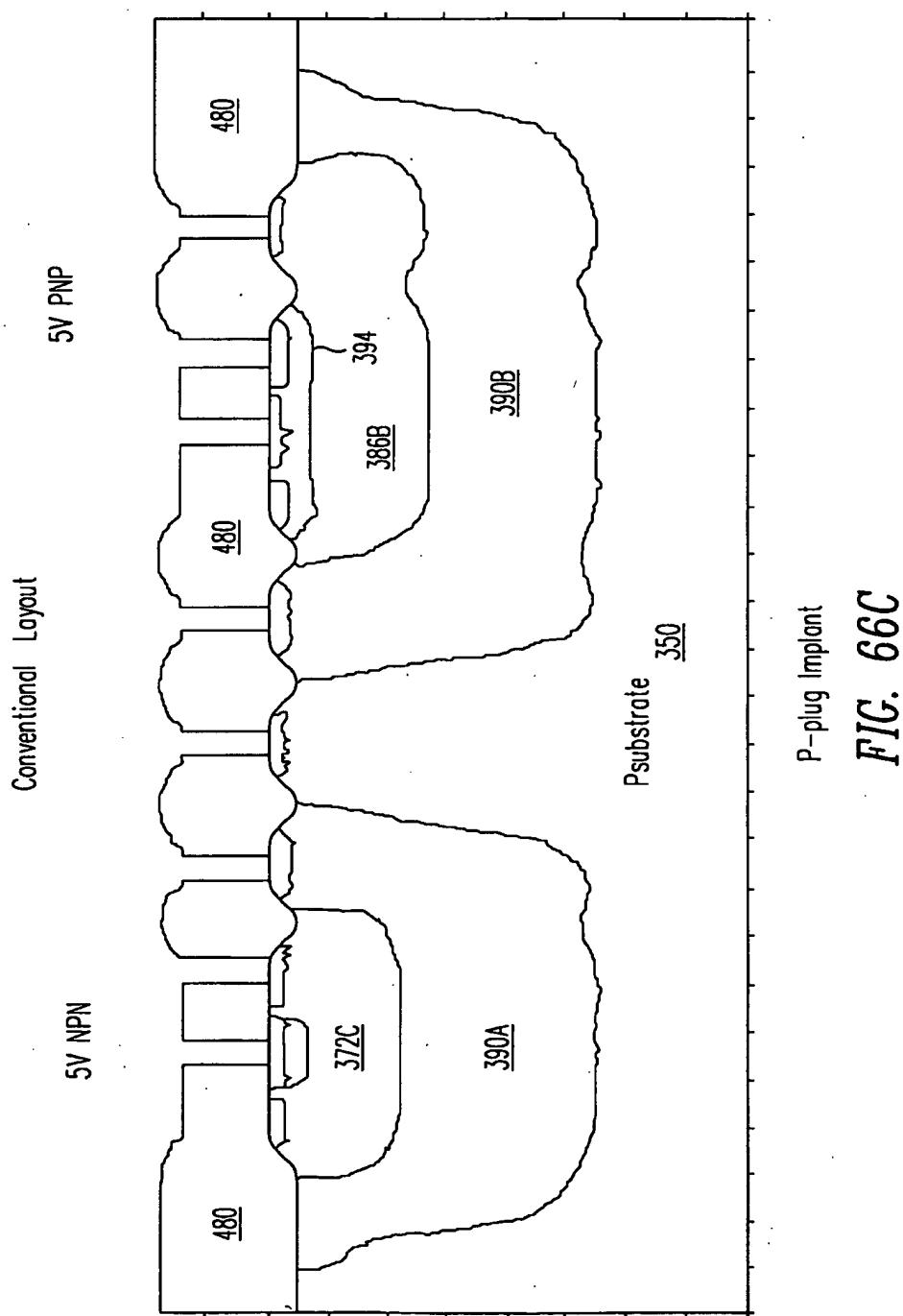
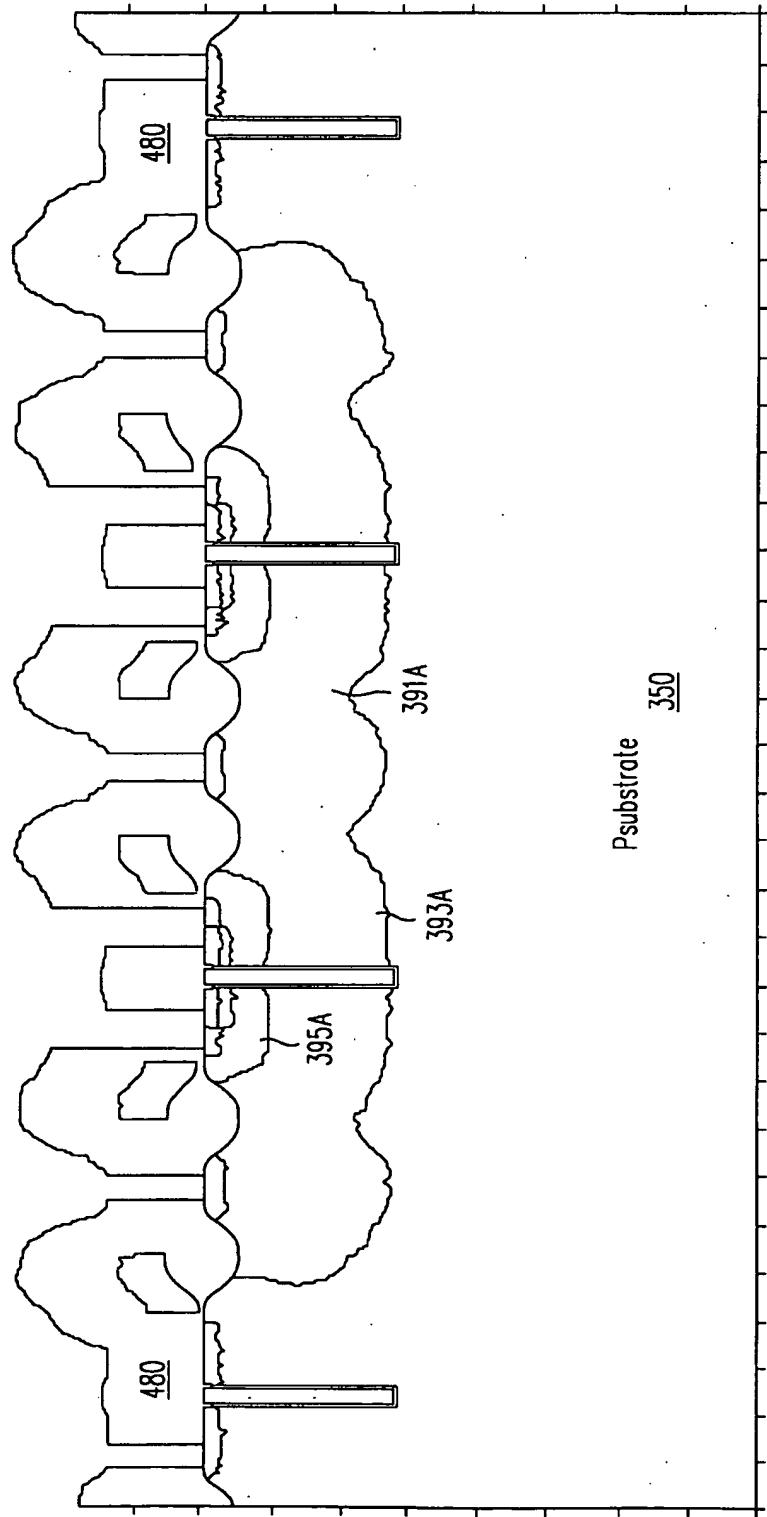


FIG. 66C

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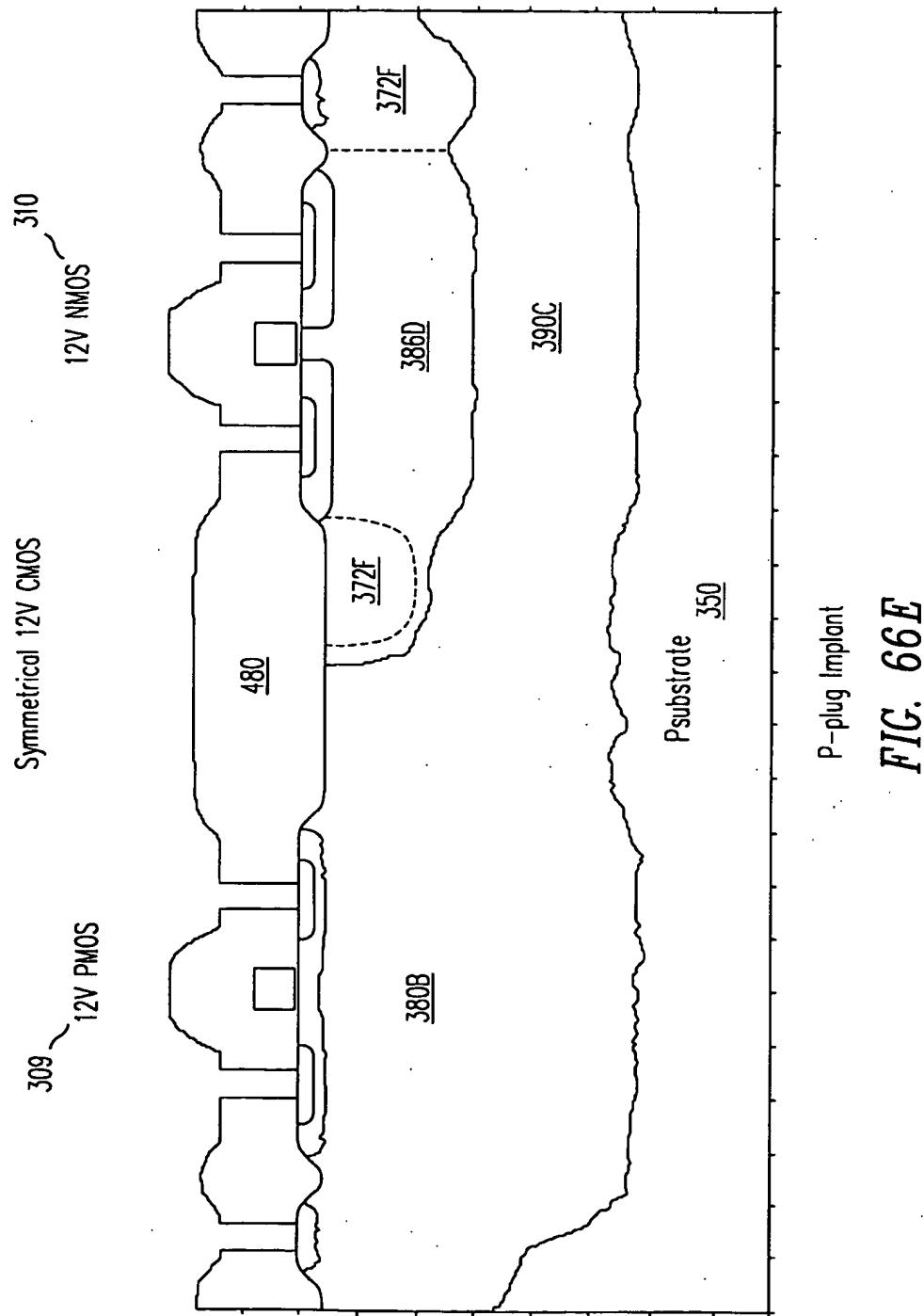
30V Lateral Trench DMOS ~ 308



P-plug implant

FIG. 66D

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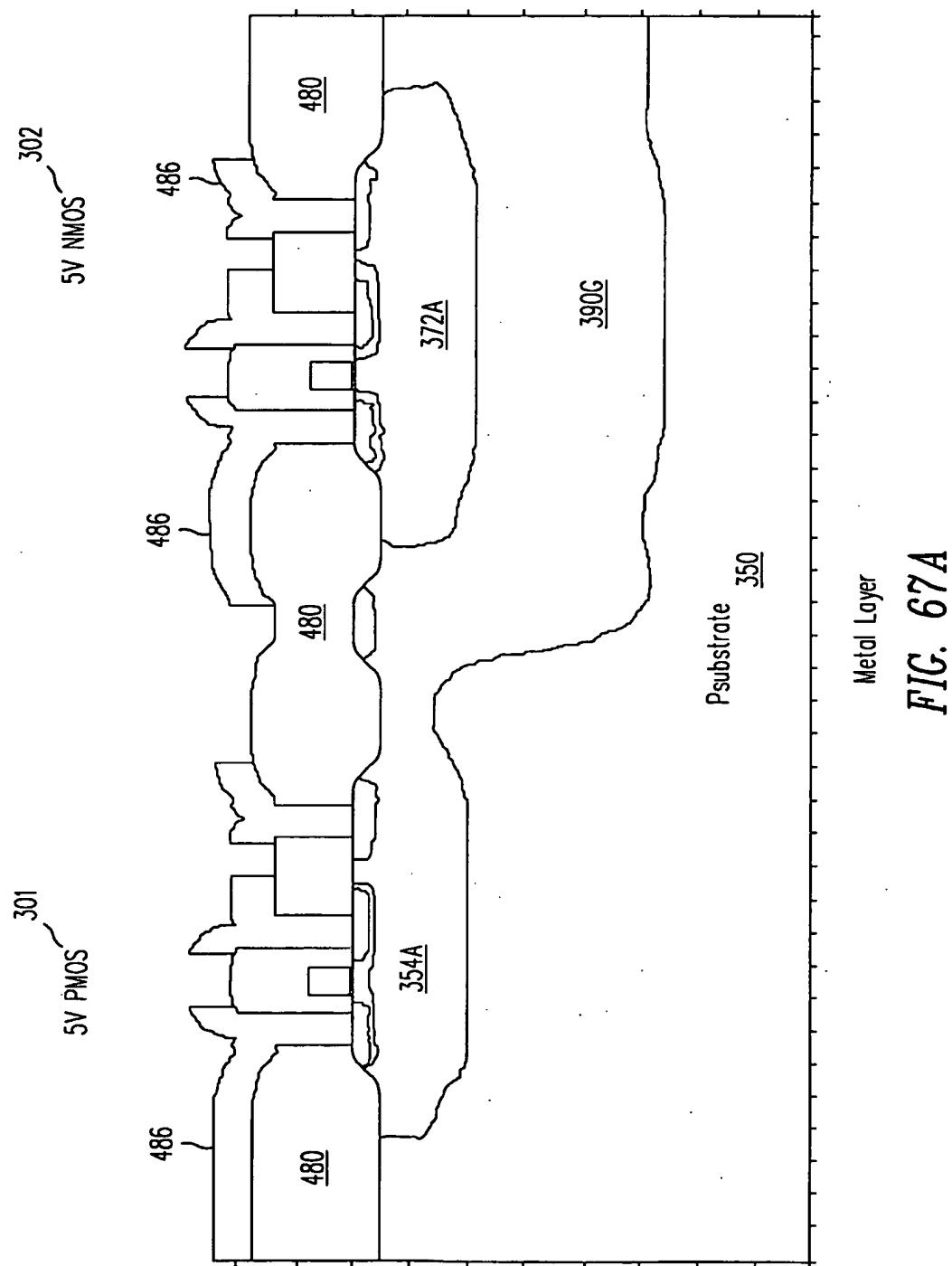


FIG. 67A

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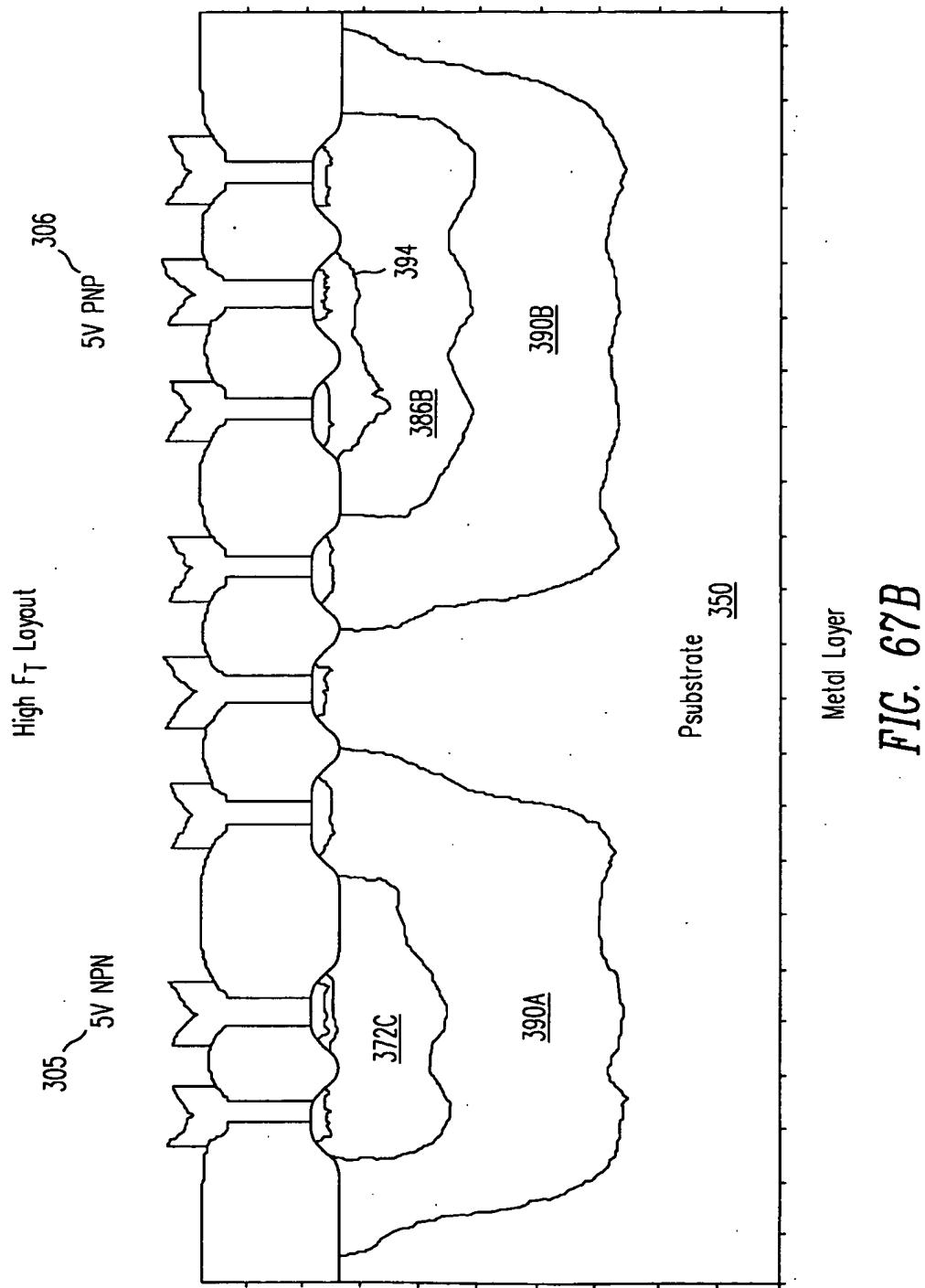
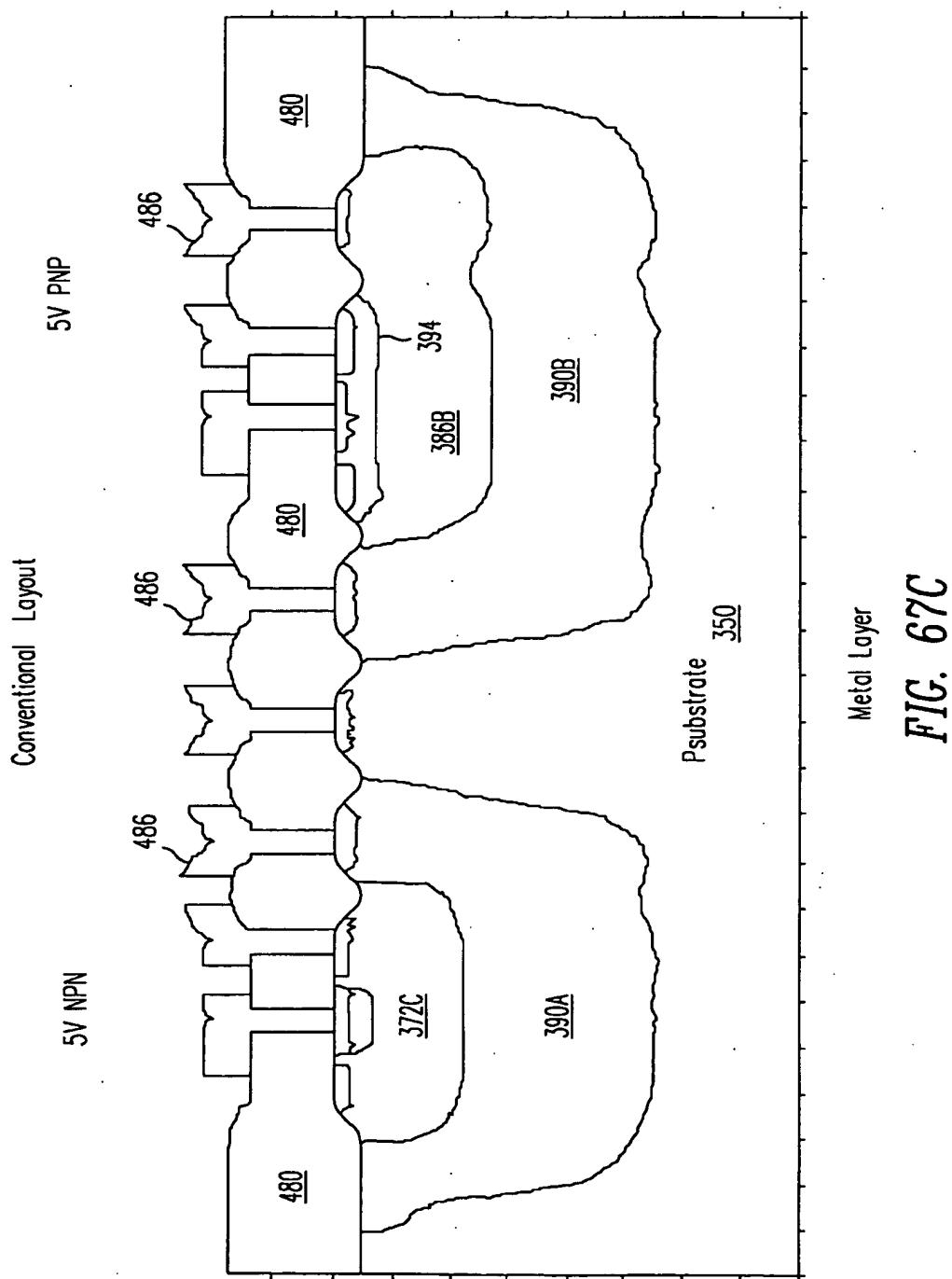


FIG. 67B



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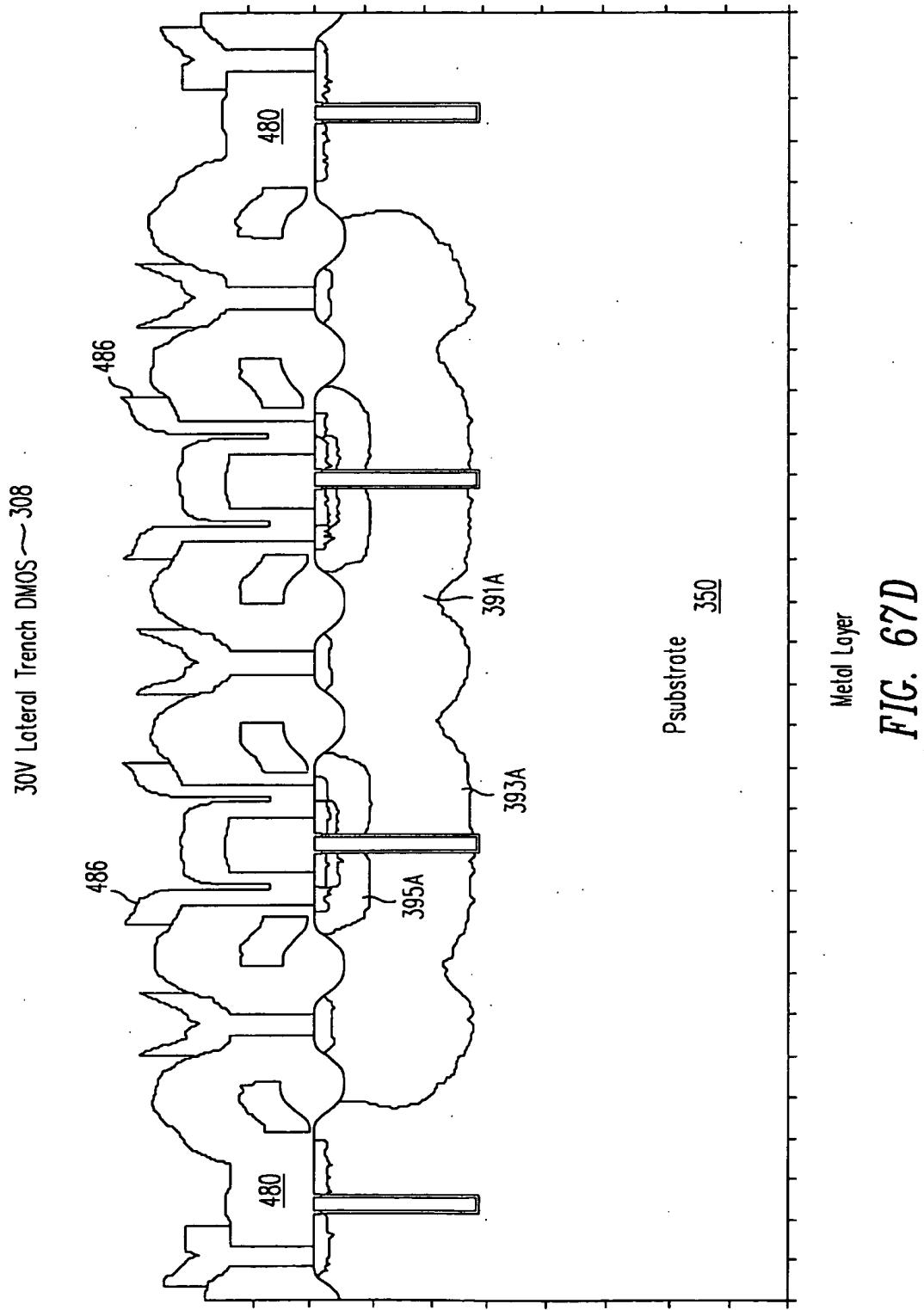


FIG. 67D

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